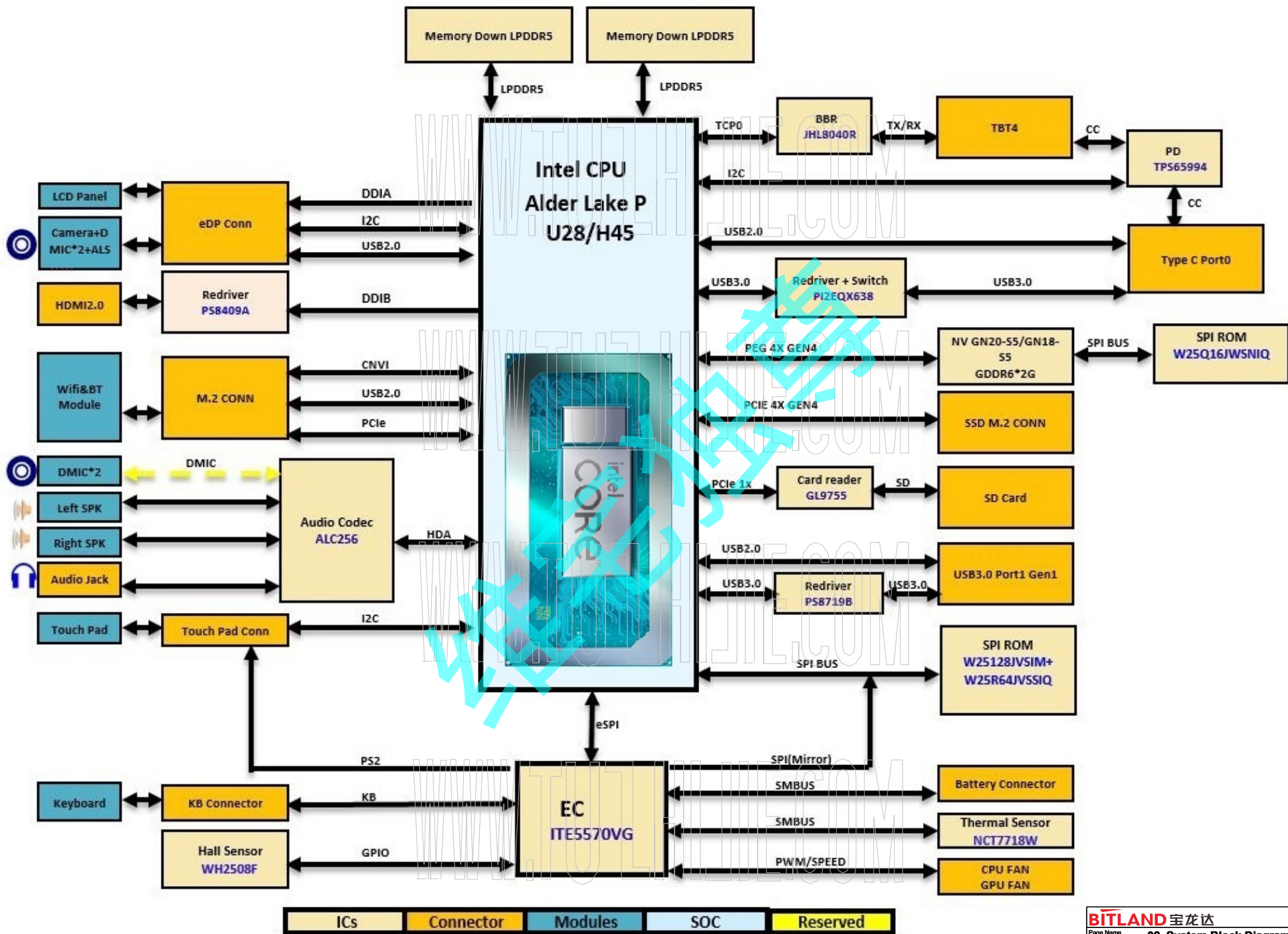


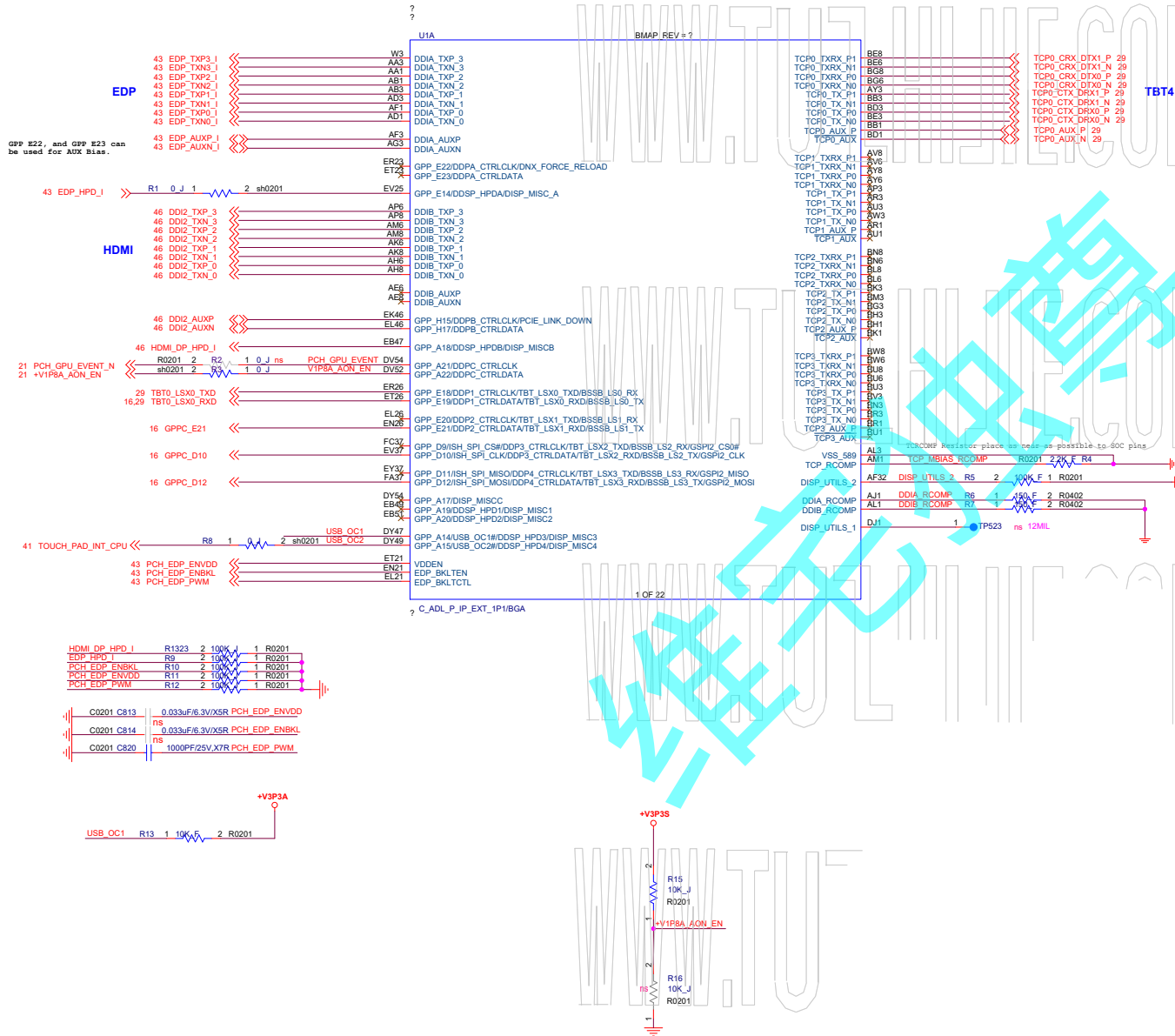
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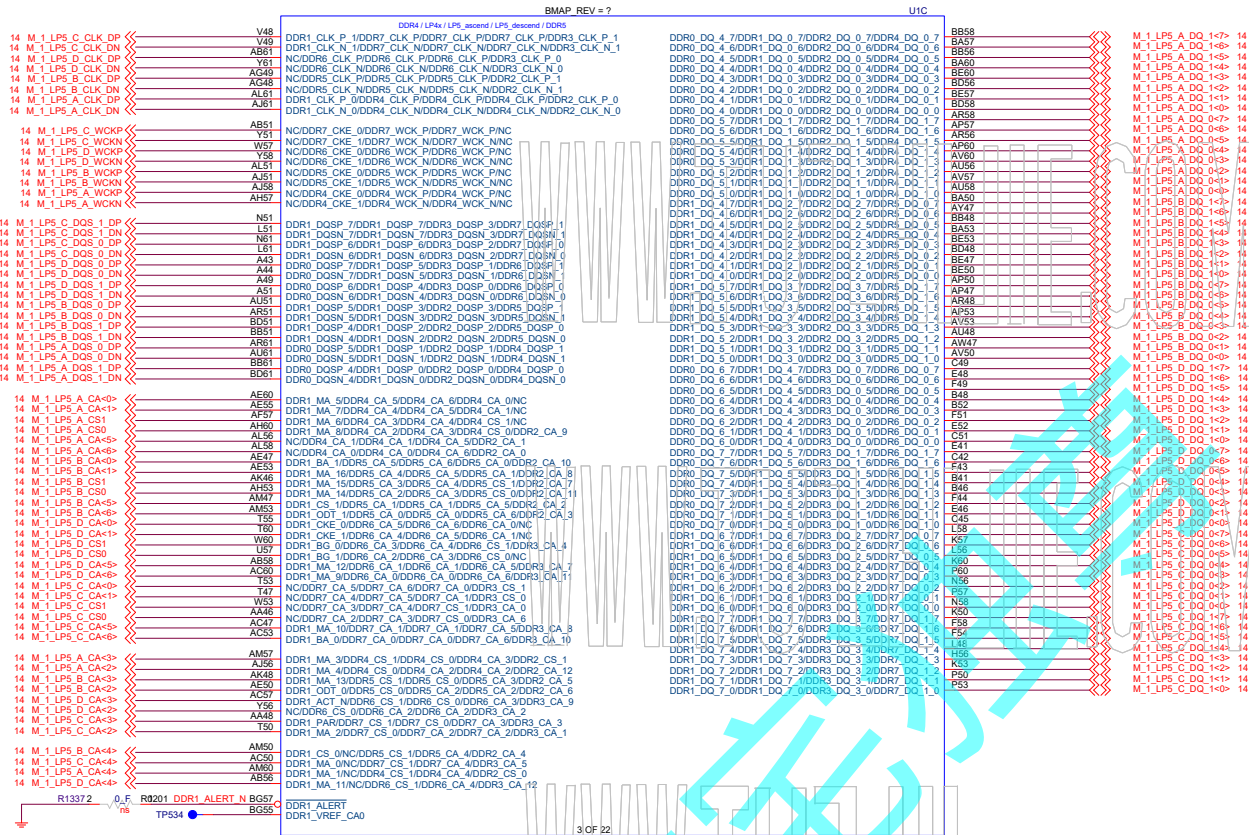
M/B Schematics Document

Intel Comet Alder-P Platform with LPDDR54+NV GN20-S5/GN18-S5 GPU

01	Title and Content	37	EC_IT5570
02	System Block Diagram	38	JWLAN/BT
03	Dispaly	39	CODEC ALC256
04	MEMORY A	40	Speaker/Audio conn
05	MEMORY B	41	TP
06	SPI/UART	42	FAN/THERMAL SENSOR
07	PCIE/USB	43	JLCD/Camera/HALL SENSOR
08	CNVI/HDA	44	KB
09	CLK	45	NA
10	CPU POWER	46	HDMI CONN
11	CPU GND	47	SFF DEBUG
12	DEBUG/RVSD	48	MB IO BOARD
13	LPDDR5_CHA	49	Nut& Hole
14	LPDDR5_CHB	50	NA
15	CPU POWER DECOUP	51	NA
16	CPU STRAPS	52	PWR_DCIN/BATT CONN
17	LPDDR5 POWER DECOUP	53	PWR_CHARGE BQ25710
18	GPU Discharge	54	PWR System 3V/5V
19	GPU_PEX	55	PWR V1P8A/S
20	GPU_IFPABCDE	56	PWR PROC1P8/1P05
21	GPU_MISC	57	PWR LPDDR5 NB66BC
22	GPU_Strap/ROM/XTA	58	PWR CPU CORE
23	GPU_NVVDD/FBVDDQ	59	PWR VCCIN AUX
24	GPU_GND	60	PWR GN20 NVDDQ RT8843
25	GPU_MEMORY_PAB	61	PWR GN20 FBVDDQ
26	NA	62	PWR V5P0A/V3P3A
27	GPU_VRAM1	63	Power Sequence
28	GPU_VRAM2	64	SUB DB IO BOARD
29	TBT_PCIE/DP	65	JTYPEC2 Retimer (PI2EQ638)
30	TBT PWR/SMIC/ROM	66	JTYPEC2 CONN
31	TBT PD TPS65994	67	DB USB3.0
32	JTYPEC1 CONN	68	NA
33	NA		
34	NA		
35	NA		
36	JSSD1		







U6 A BYTE1

U6 A BYTE0

U6 B BYTE1

U6 B BYTE0

U7 D BYTE1

U7 D BYTE0

U7 C BYTE0

U7 C BYTE1

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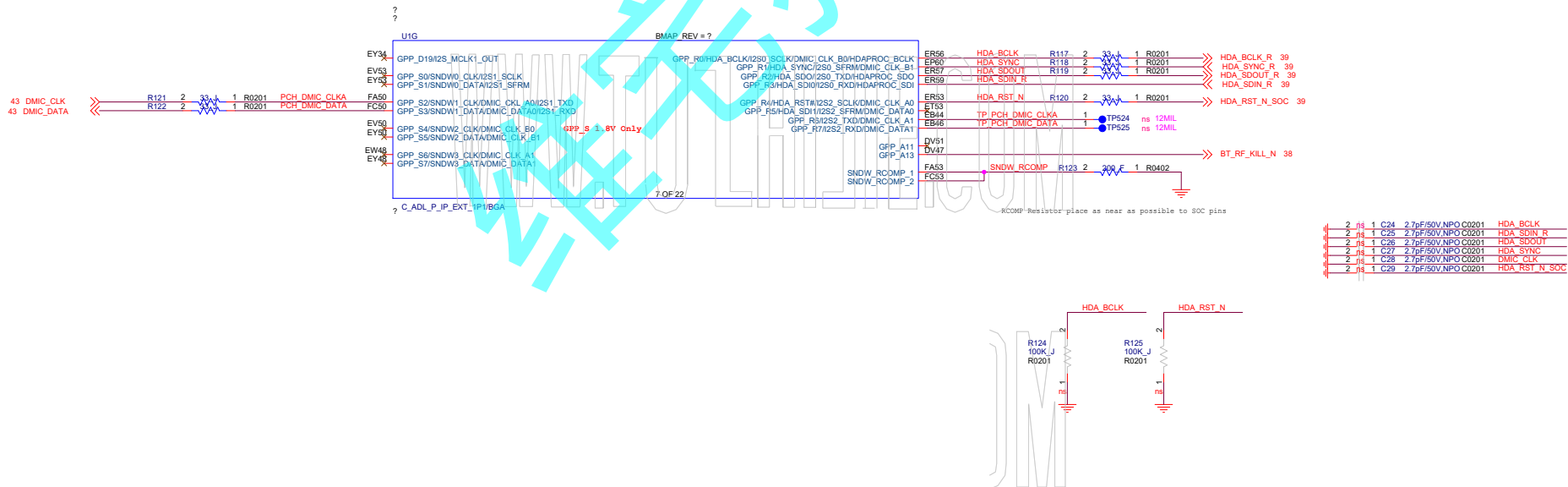
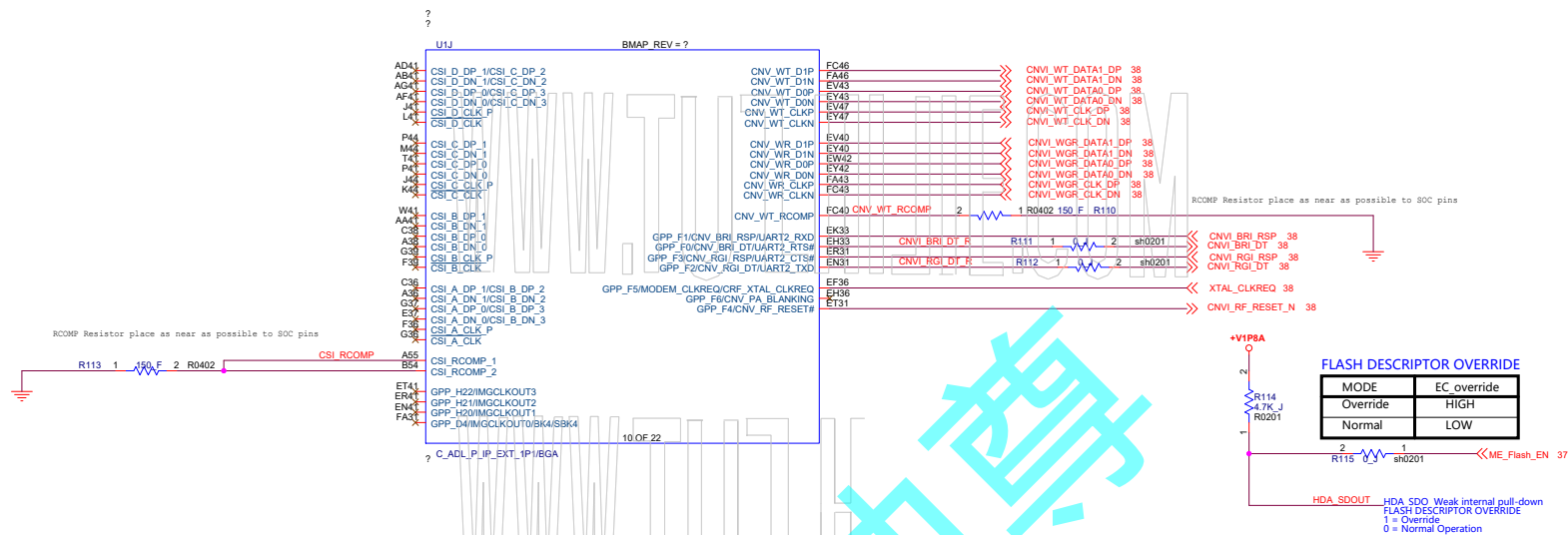
Page Name
MEMORY B

Size C Project Name A28&A39 Rev V1.0

Date: Wednesday, October 20, 2021 Sheet 5 of 68

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Page Name		CNV/HDA	
Size	Project Name	A28&A39	
C			Rev V1.0
Date: Monday, December 13, 2021		Sheet	8 of 68
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<ul style="list-style-type: none"> CLKOUT_PCIE_P [6:0] CLKOUT_PCIE_N [6:0] 	0	Yes	<p>PCI Express® Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices</p> <ul style="list-style-type: none"> CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support <p>Any on-board CLKOUT_PCIE_P/N differential pair not being routed on a platform should be configured as "Disabled" through the Intel® Flash Image Tool (FIT) tool. The CLKOUT_PCIE_P/N differential pairs are called out as CLKOUT_SRC differential outputs in FIT as discussed in the SPI Programming Guide.</p>
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SSD1
GPU
WLAN
SD

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PCIE_CLK_SSD1_DP
PCIE_CLK_SSD1_DN
PCIE_CLK_GPU_DP
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PCIE_CLK_SSD1_DP
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PCIE_CLK_SSD1_DP
PCIE_CLK_SSD1_DN
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PCIE_CLK_SSD1_DP
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PCIE_CLK_SSD1_DP
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PCIE_CLK_SSD1_DP
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PCIE_CLK_SSD1_DP
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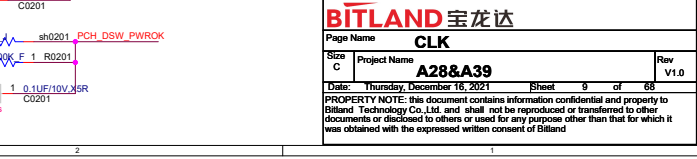
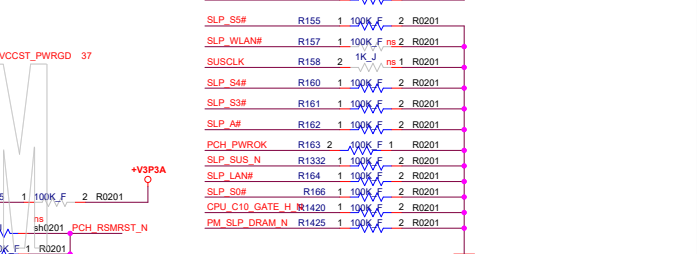
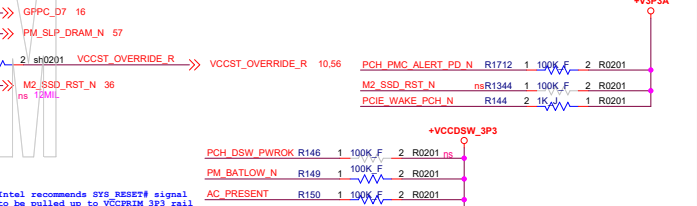
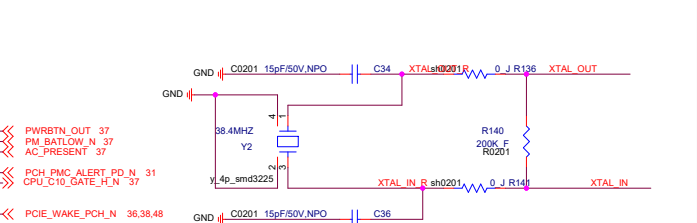
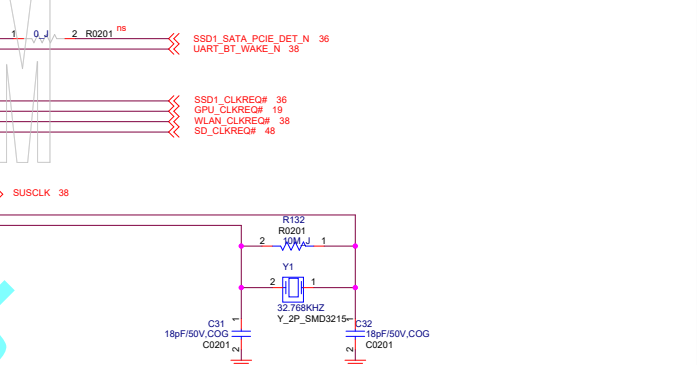
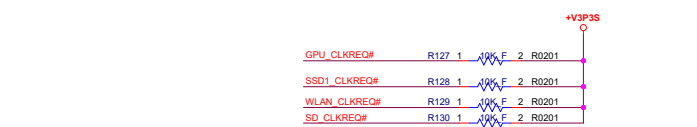
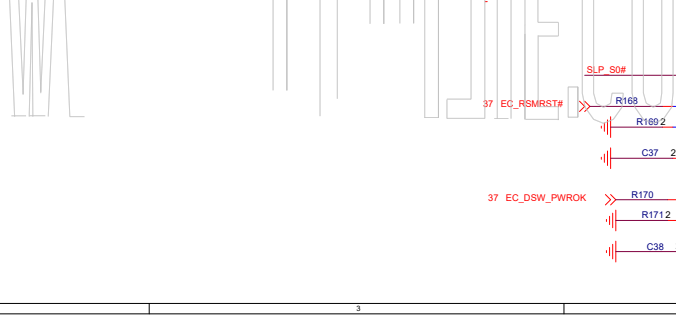
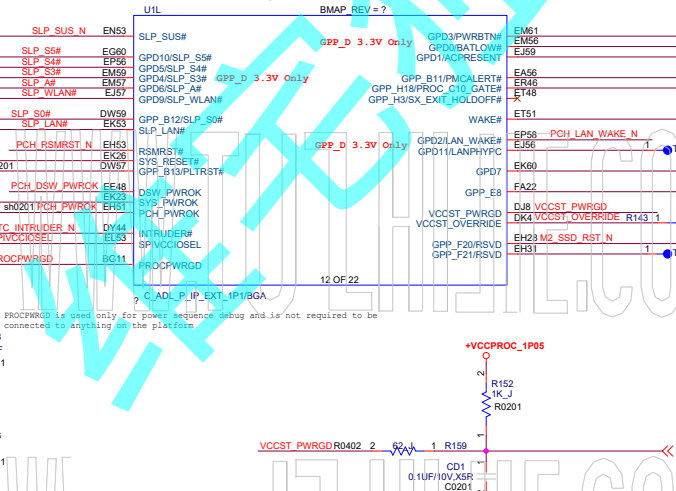
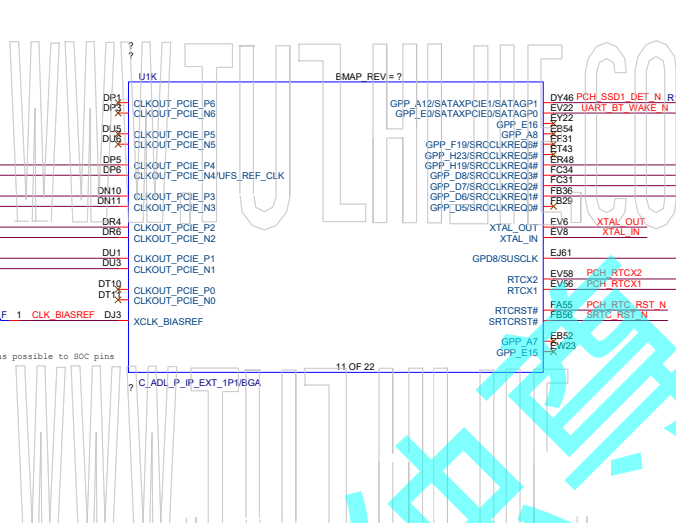
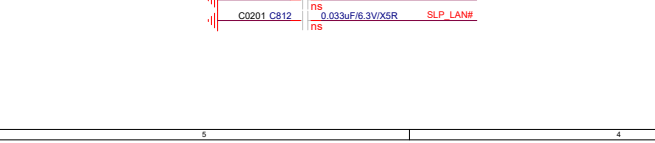
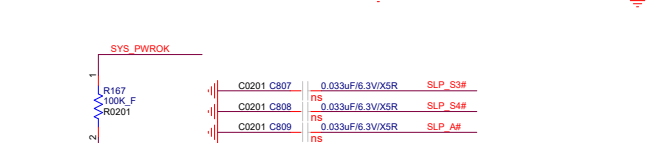
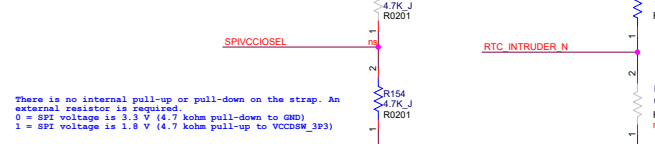
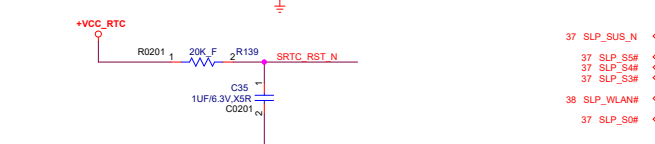
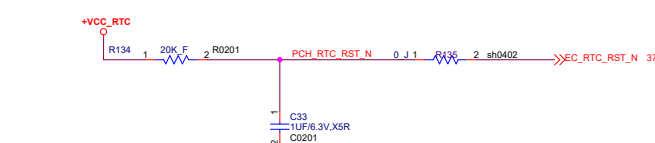
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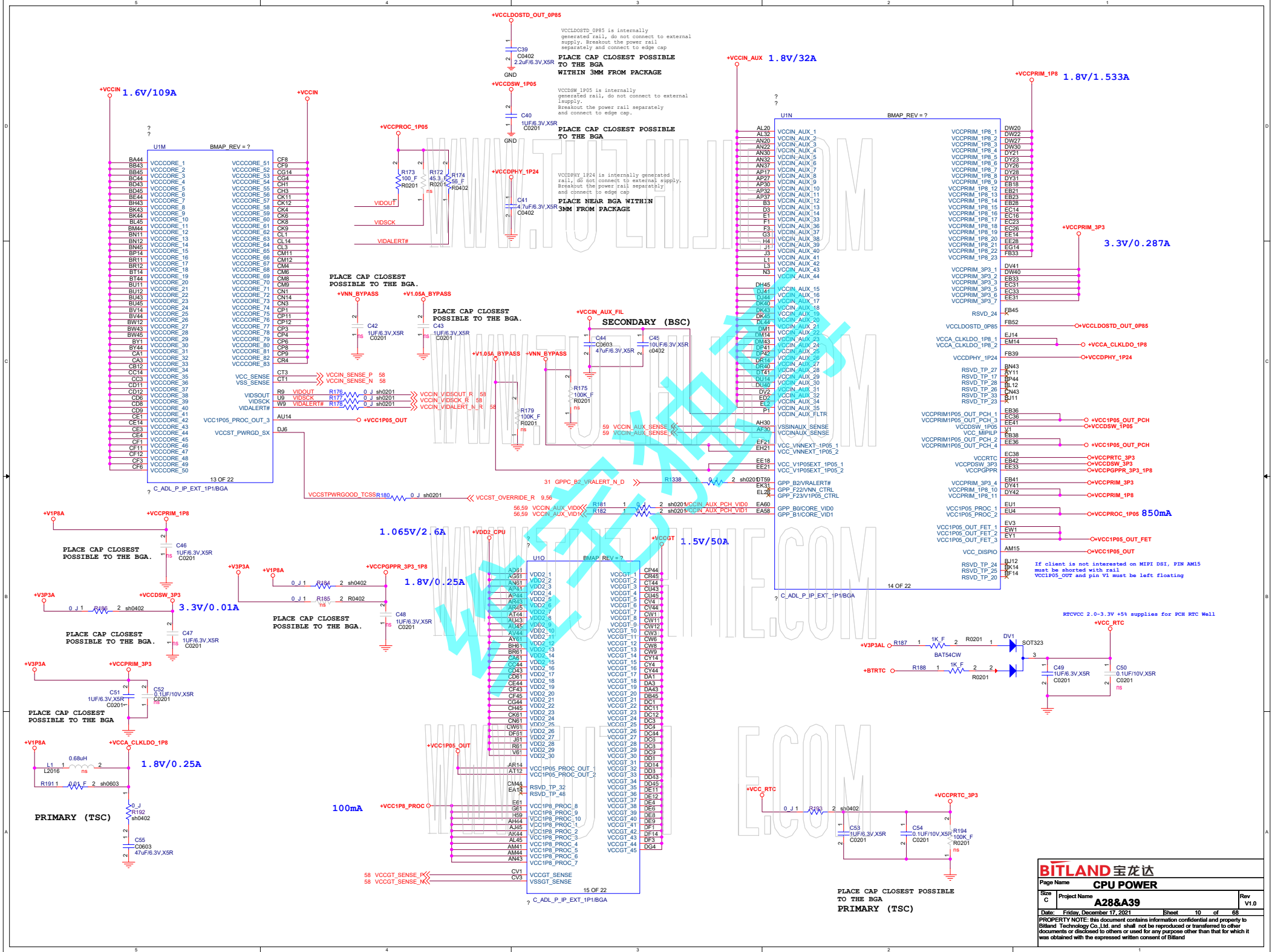
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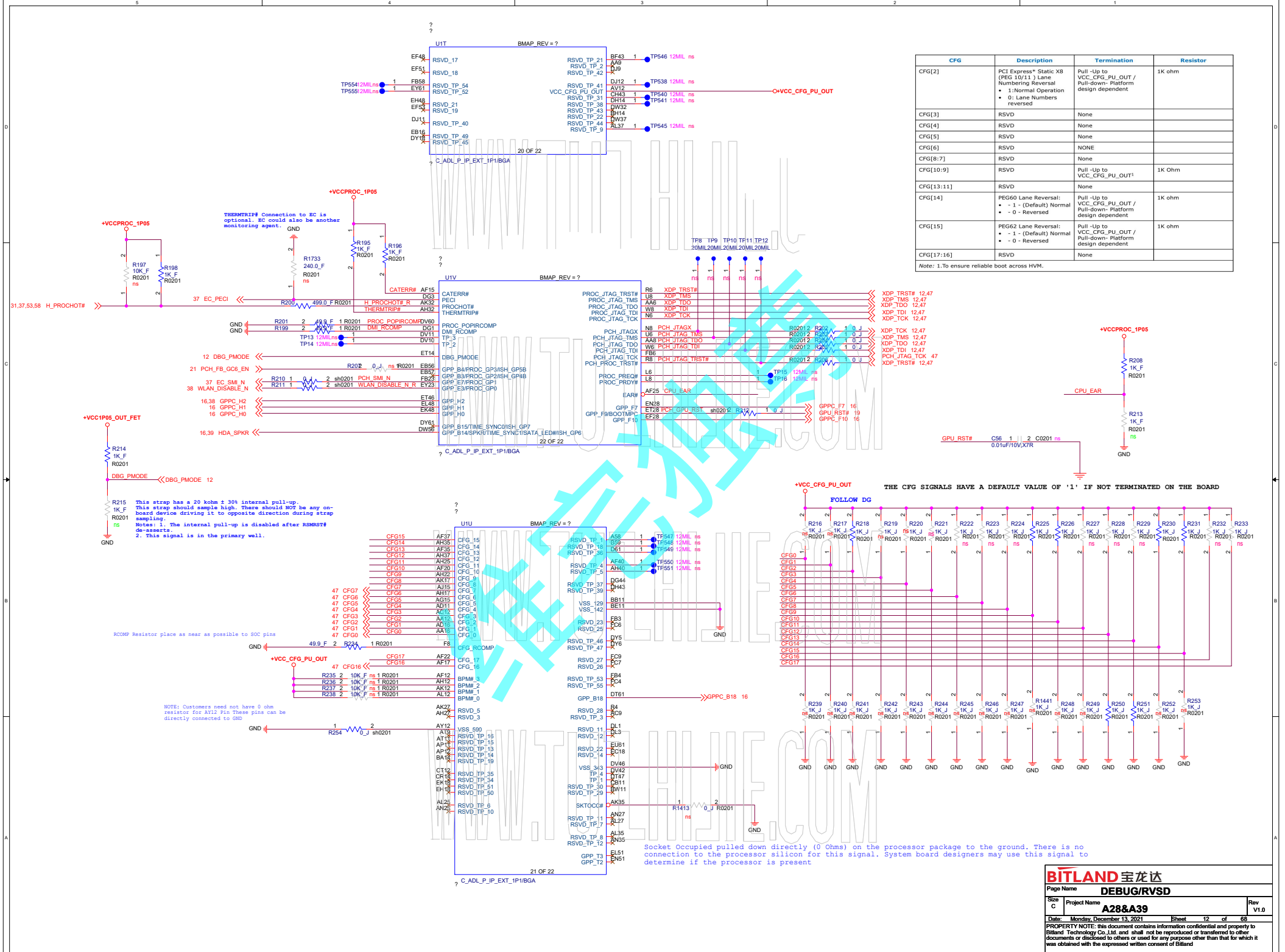
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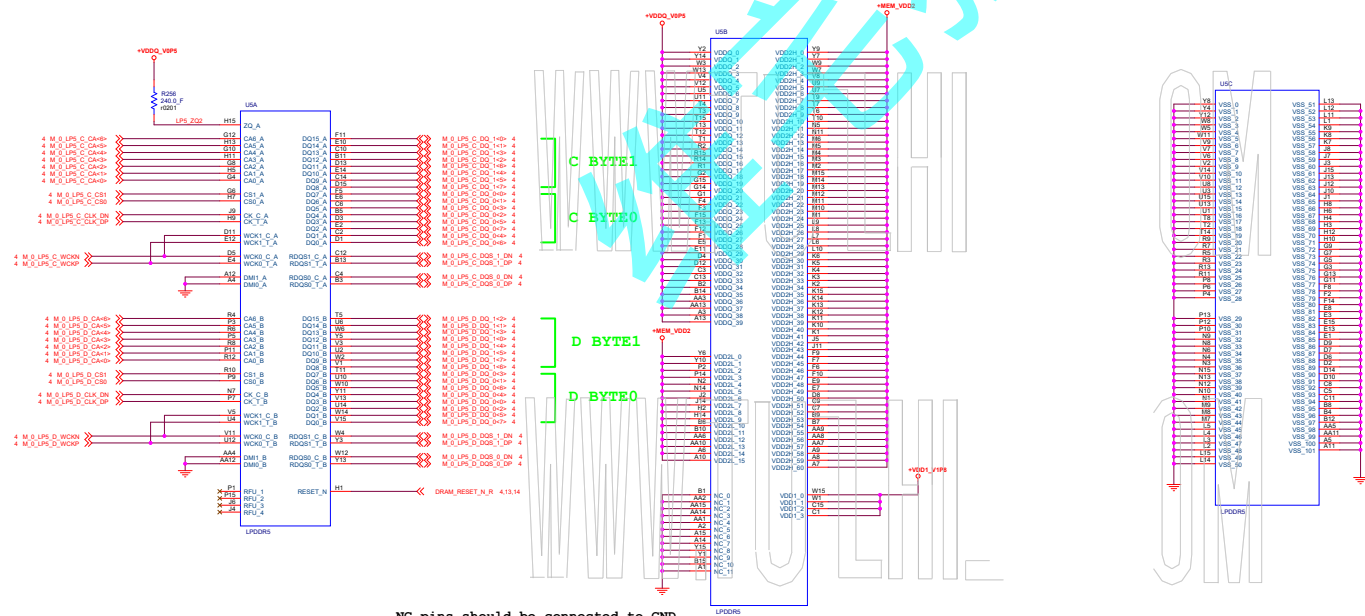
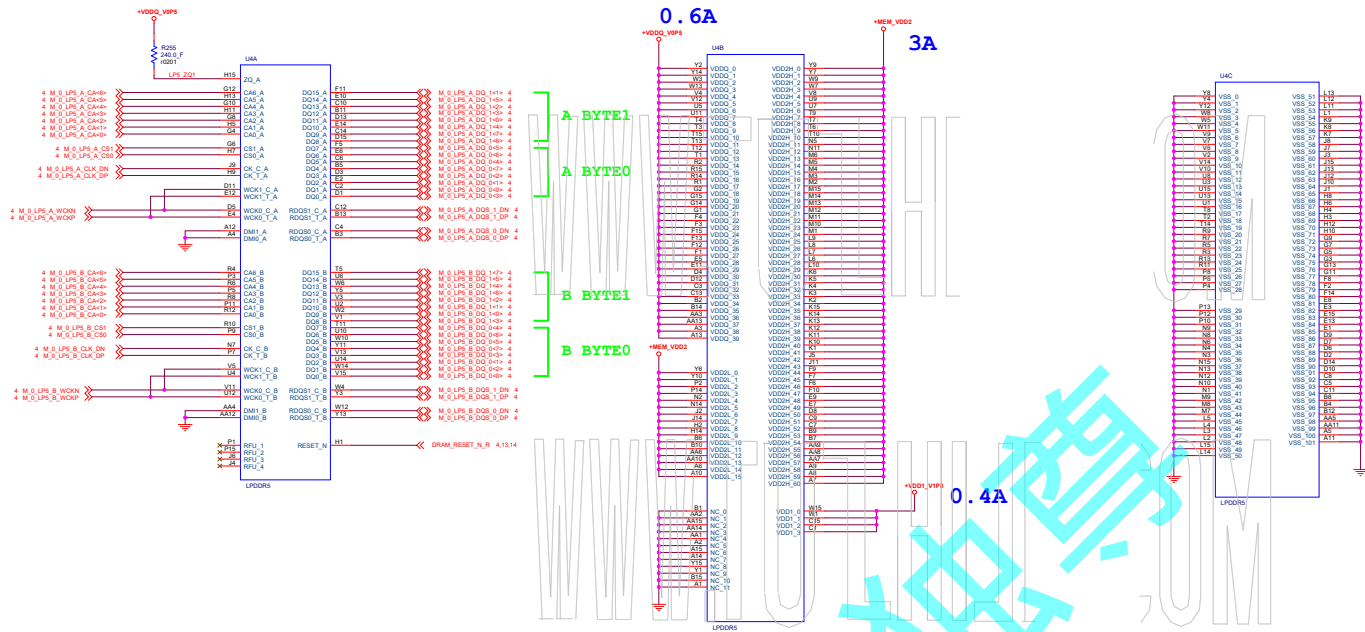
CFG	Description	Termination	Resistor
CFG[2]	PCI Express* Static X8 (PEG 10/11) Lane Numbering Reversal • - 1: Normal Operation • - 0: Lane Numbers reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down: Platform design dependent	1K ohm
CFG[3]	RSVD	None	
CFG[4]	RSVD	None	
CFG[5]	RSVD	None	
CFG[6]	RSVD	NONE	
CFG[8:7]	RSVD	None	
CFG[10:9]	RSVD	Pull -Up to VCC_CFG_PU_OUT ¹	1K Ohm
CFG[13:11]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down: Platform design dependent	1K ohm
CFG[15]	PEG62 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down: Platform design dependent	1K ohm
CFG[17:16]	RSVD	None	

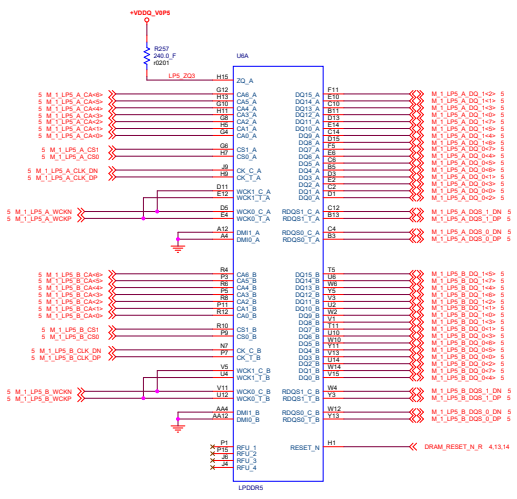
Note: 1.To ensure reliable boot across HVM.

THE CFG SIGNALS HAVE A DEFAULT VALUE OF '1' IF NOT TERMINATED ON THE BOARD

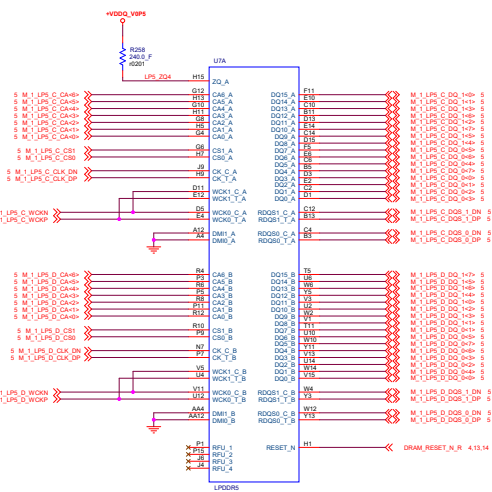
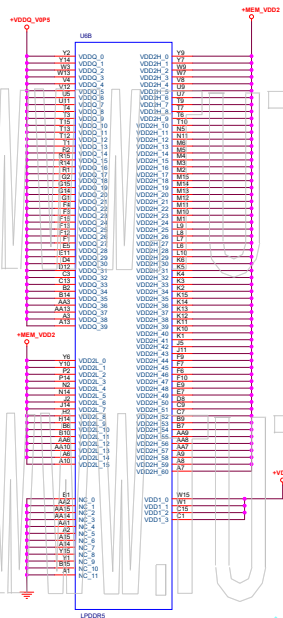
FOLLOW DG

Socket Occupied pulled down directly (0 Ohms) on the processor package to the ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present

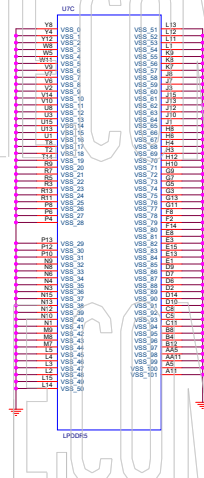
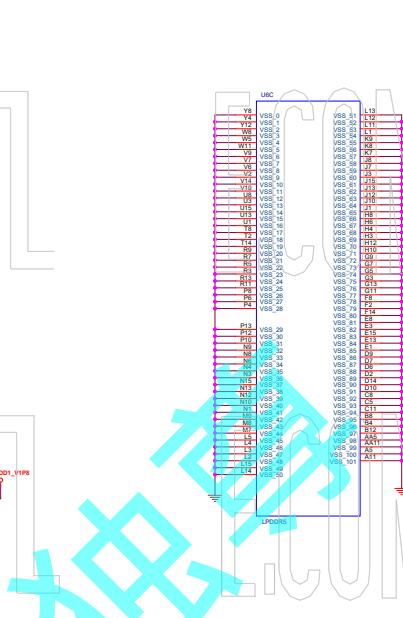
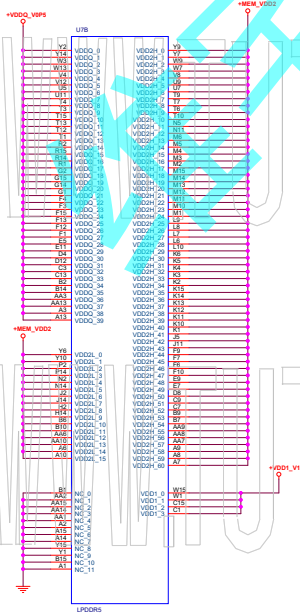


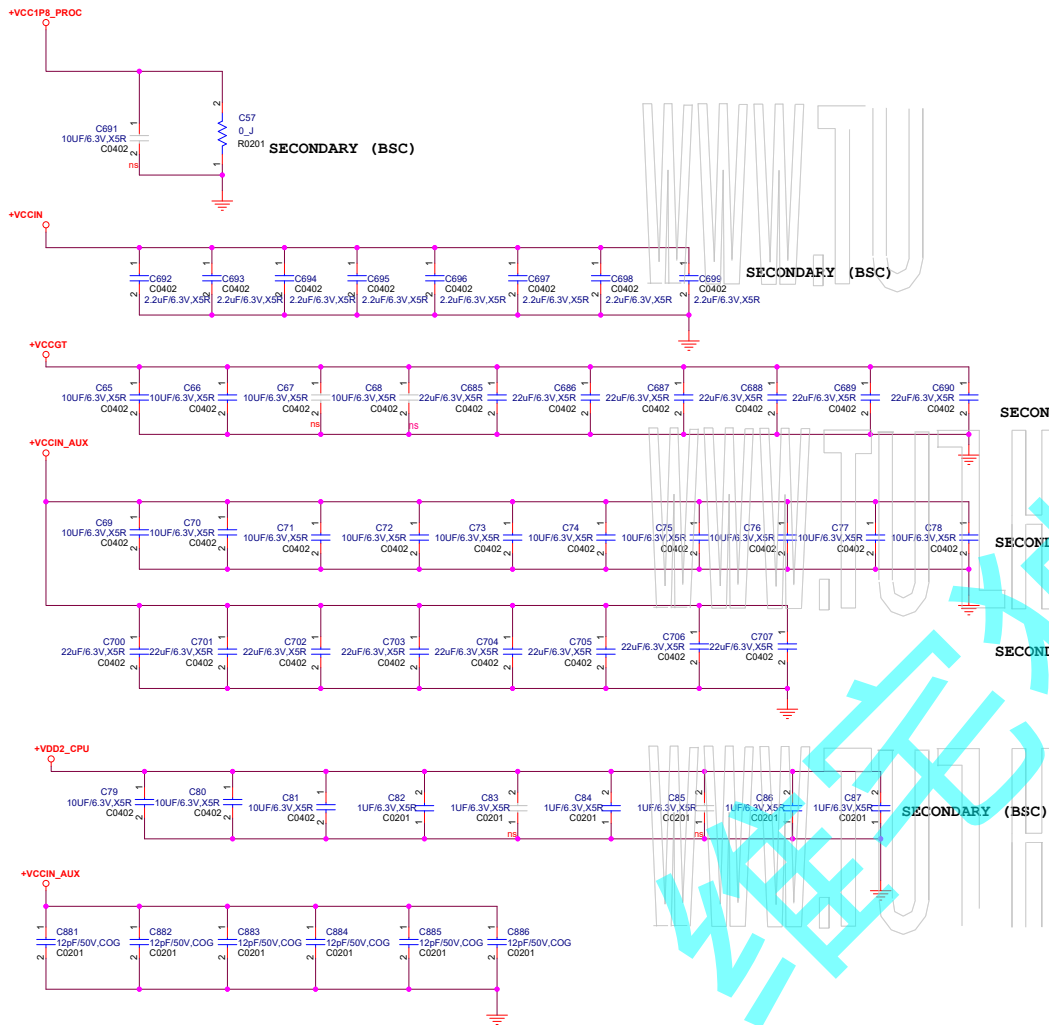


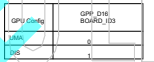
NC pins should be connected to GND

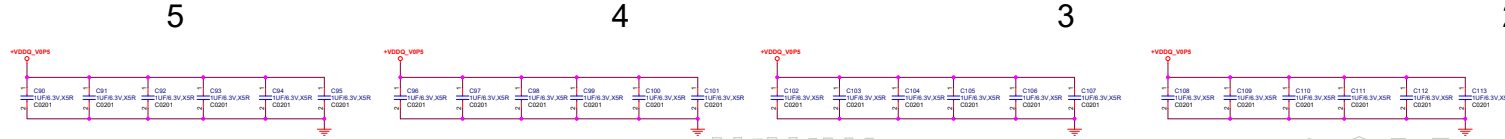


NC pins should be connected to GND



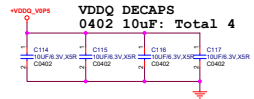




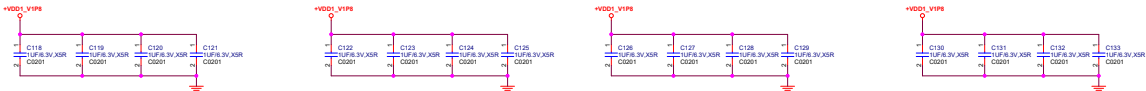


VDDQ DECAPS
0201 1uF: TOTAL 24

Distribute 6 caps per DRAM, 2 per short edge and 1 per long edge close to VDD2H/VDD2L BGA's

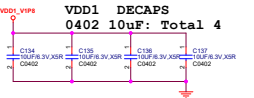


DISTRIBUTE EVENLY, 1 FOR EACH DRAM MODULE



VDD1 DECAPS
0201 1uF: TOTAL 16

DISTRIBUTE EVENLY, 4 CAPS PER DRAM, 2 PER LONG EDGE CLOSE TO VDD1 BGA'S

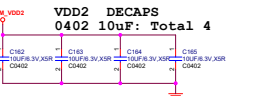


DISTRIBUTE EVENLY AMONG ALL DRAMS

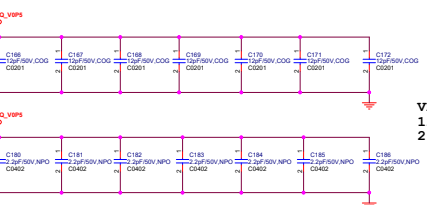


VDD2 DECAPS
0201 1uF: TOTAL 24

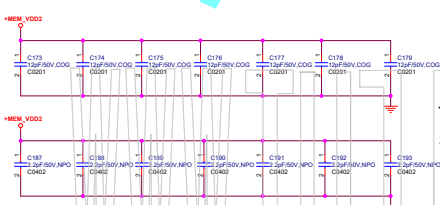
DISTRIBUTE EVENLY, 6 caps per DRAM, 2 per short edge and 1 per long edge close to VDD2H/VDD2L BGA's



DISTRIBUTE EVENLY AMONG ALL DRAMS



VDDQ EMC CAPS
12PF: Total 7
2.2PF: Total 7



VDD2 EMC CAPS
12PF: Total 7
2.2PF: Total 7

Distribute evenly less than 4mm apart from DRAM and less than 12 mm gap between each pair (12pf adn 2.2pf) of capacitor.

Distribute evenly less than 4mm apart from DRAM and less than 12 mm gap between each pair (12pf adn 2.2pf) of capacitor.

D

D

C

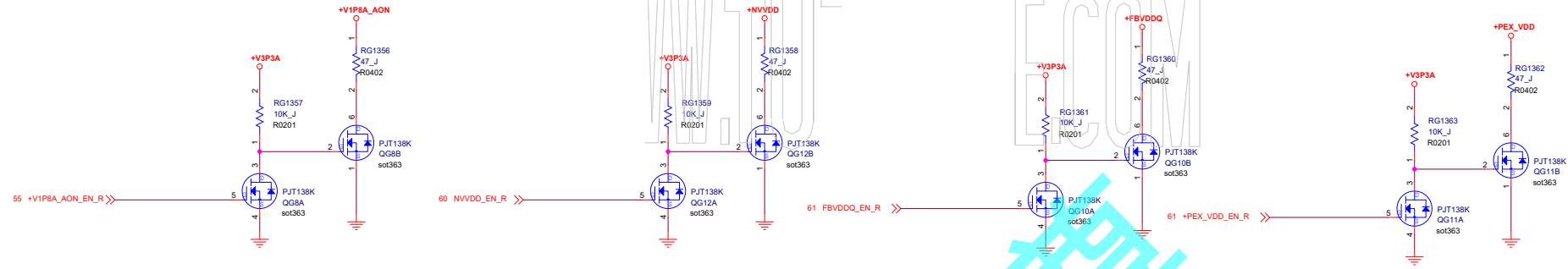
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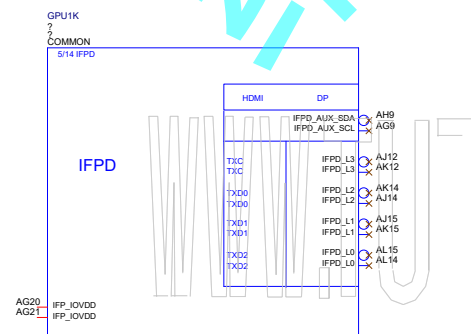
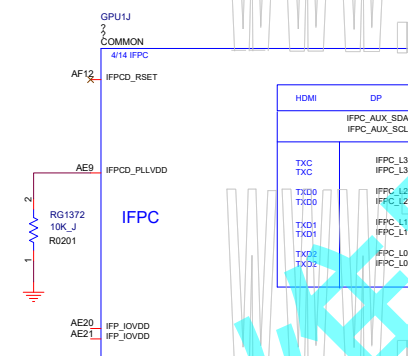
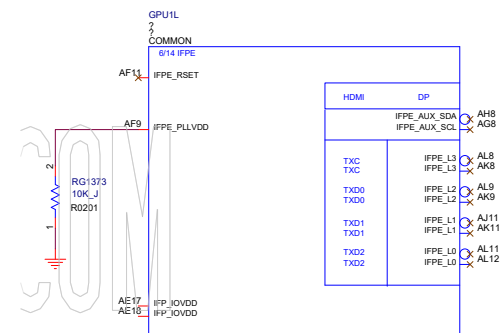
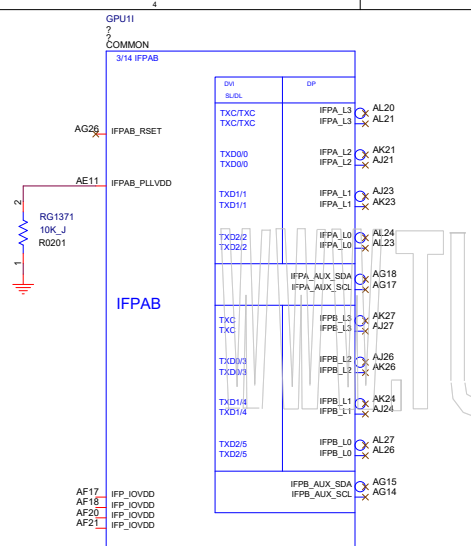
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B

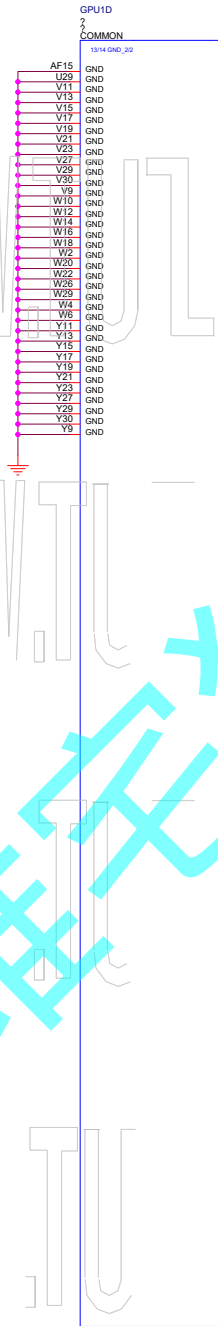
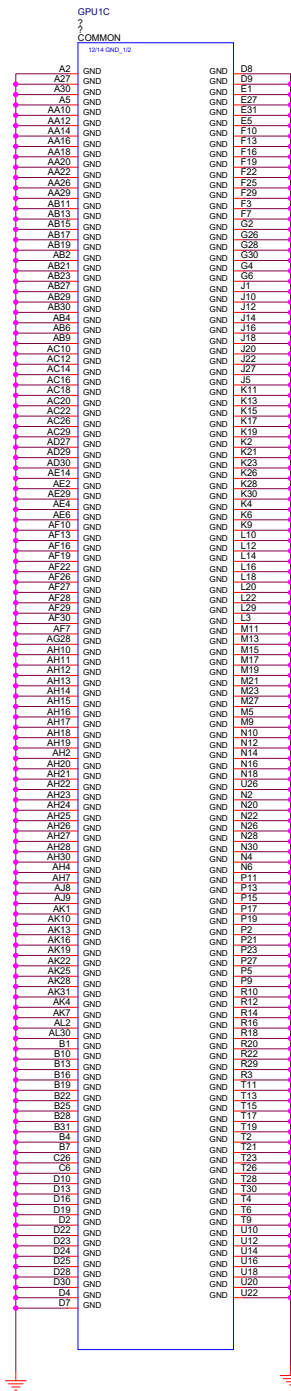
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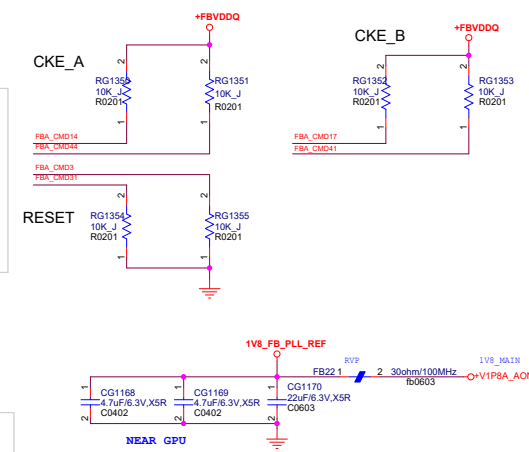
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Page Name			
GPU MEMORY PAB			
Size	Project Name	Rev	
C	A28&A39	V1.0	
Date:	Wednesday, October 20, 2021	Sheet	25 of 68

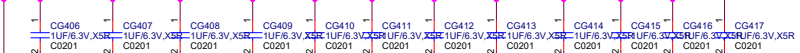
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RVP:
1.CLOSE OR UNDER DRAM:1u*18+10u*4
2.Around:22u*6+10uf*2

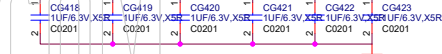
DECOUPLING FOR ONE DRAM

PLACE 0201 1UF UNDER MEMORY AS MUCH AS POSSIBLE

CLOSE OR UNDER DRAM



CLOSE OR UNDER DRAM



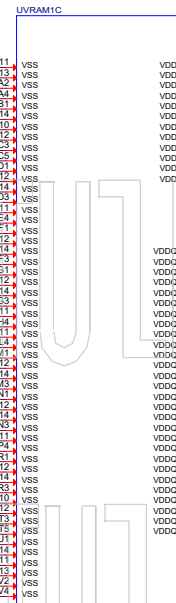
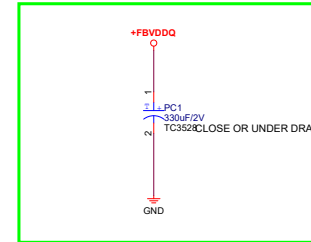
AROUND DRAM



CLOSE OR UNDER DRAM



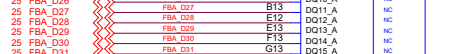
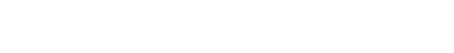
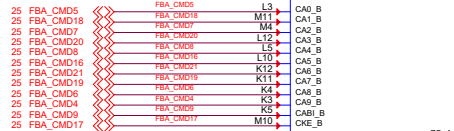
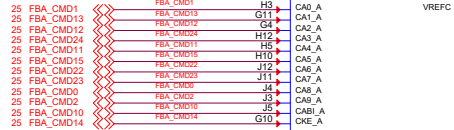
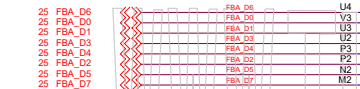
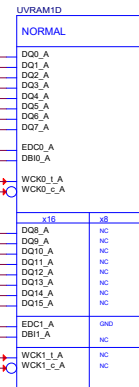
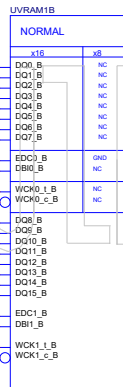
CLOSE OR UNDER DRAM



V550 #62 1.8V5_0V需要 一个posM1.8v 31uVx10

25.28 FBA_DB[7:0] << FBA_DB[7:0]

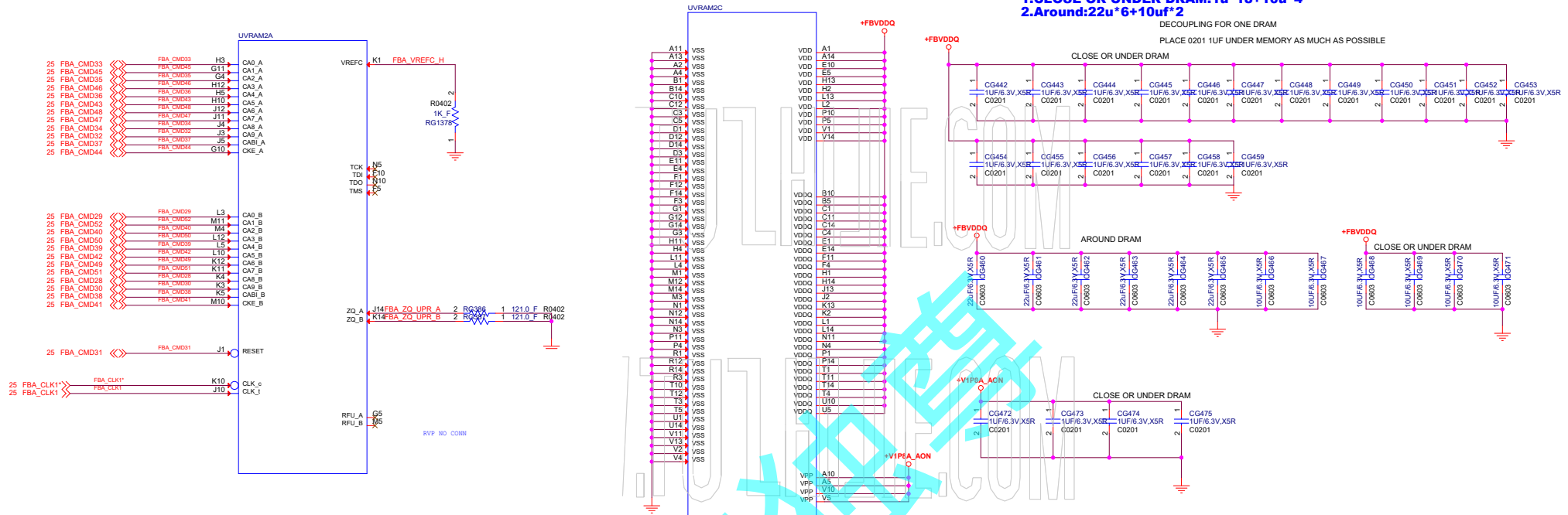
25.28 FBA_EDC[7:0] << FBA_EDC[7:0]



RVP:
1.CLOSE OR UNDER DRAM:1u*18+10u*4
2.Around:22u*6+10uf*2

DECOUPLING FOR ONE DRAM

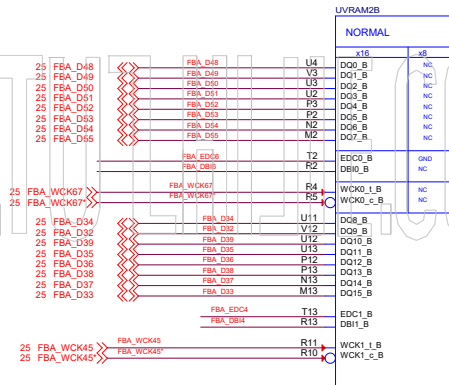
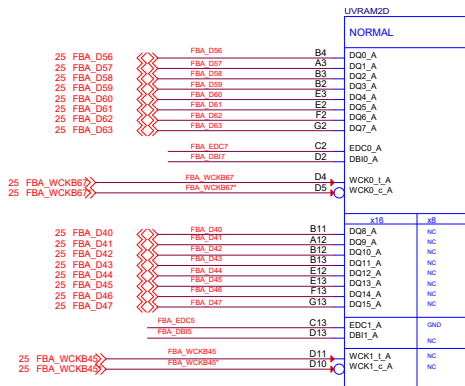
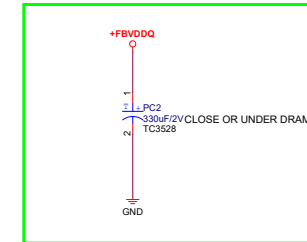
PLACE 0201 1UF UNDER MEMORY AS MUCH AS POSSIBLE

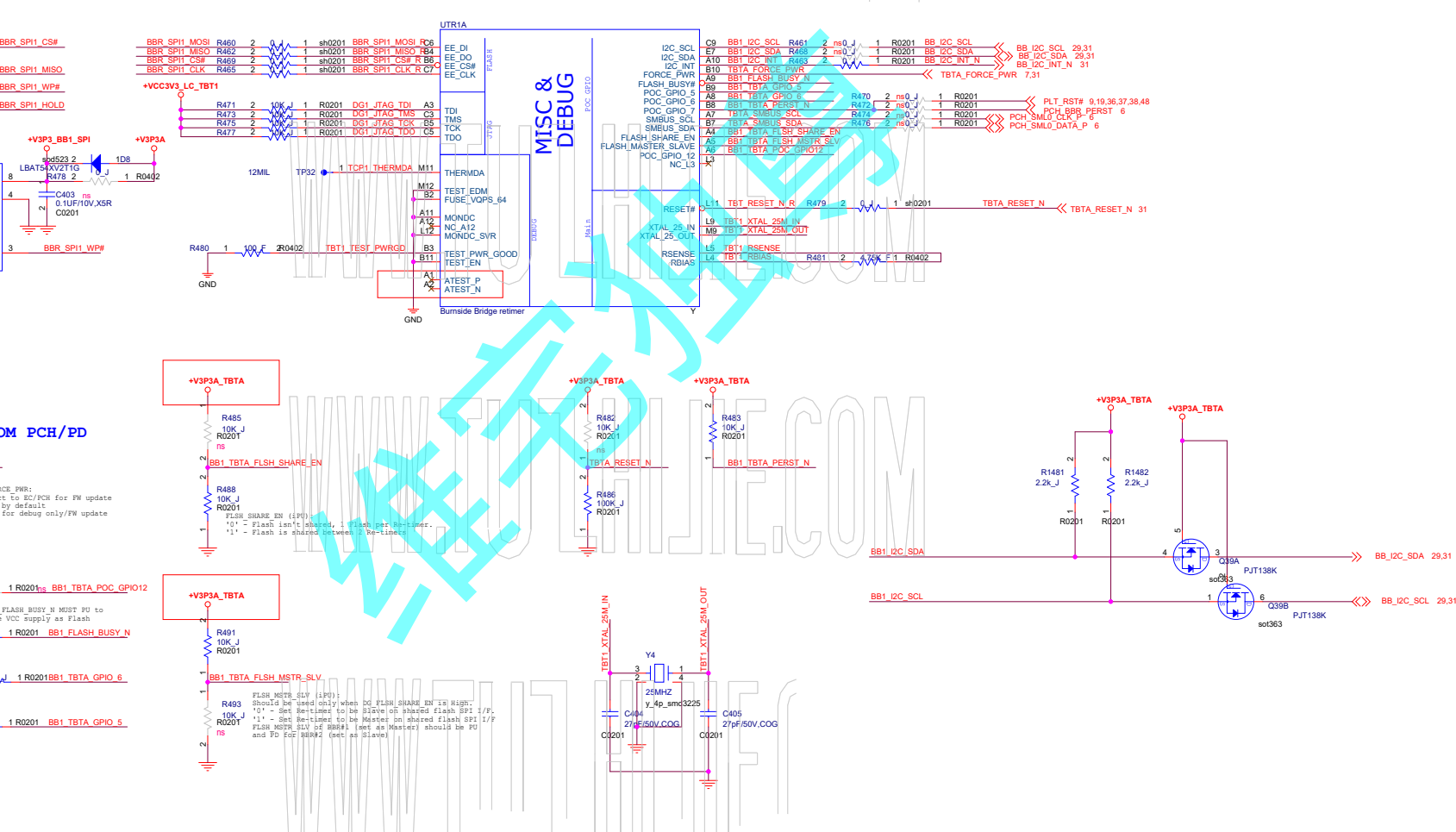


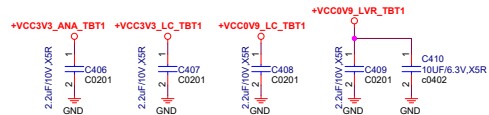
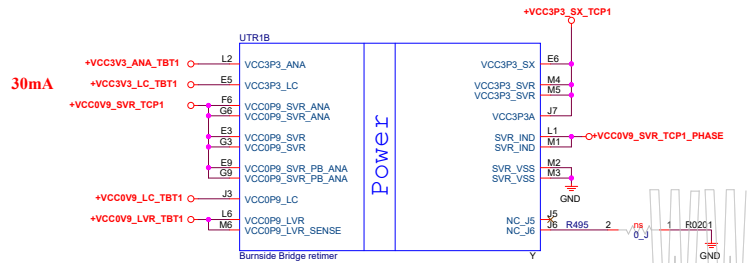
25,27 FBA_DB[7..0] << FBA_DB[7..0]

25,27 FBA_EDC[7..0] << FBA_EDC[7..0]

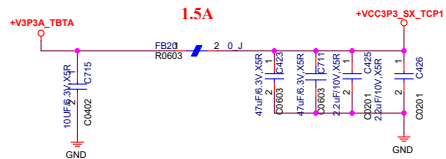
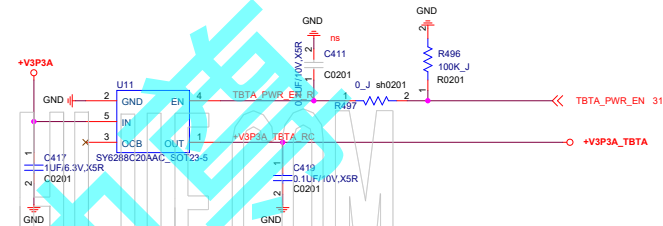
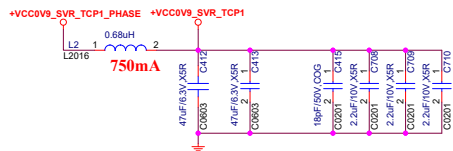
FBA_DB[0]
FBA_DB[1]
FBA_DB[2]
FBA_DB[3]
FBA_DB[4]
FBA_DB[5]
FBA_DB[6]
FBA_DB[7]
FBA_EDC[0]
FBA_EDC[1]
FBA_EDC[2]
FBA_EDC[3]
FBA_EDC[4]
FBA_EDC[5]
FBA_EDC[6]
FBA_EDC[7]



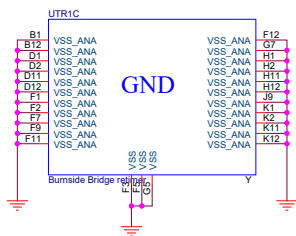




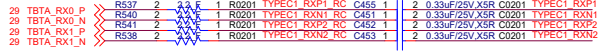
RETIMER POWER GATE



Burnside Bridge for Port 1 (GND Symbol)

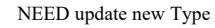
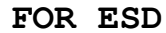


AC CAP 25V,must C0201
RX 0.33U TX 0.22U

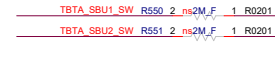
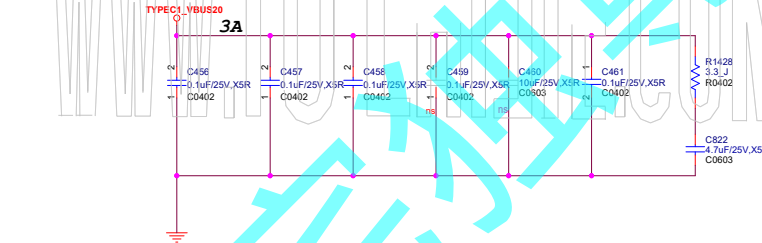


TYPEC1	TXP1	R542	1	22%	F	2	R0201
TYPEC1	TXN1	R543	1	22%	F	2	R0201
TYPEC1	TXP2	R544	1	22%	F	2	R0201
TYPEC1	TXN2	R545	1	22%	F	2	R0201
TYPEC1	RXP1	R546	1	22%	F	2	R0201
TYPEC1	RXN1	R547	1	22%	F	2	R0201
TYPEC1	RXP2	R548	1	22%	F	2	R0201
TYPEC1	RXN2	R549	1	22%	F	2	R0201

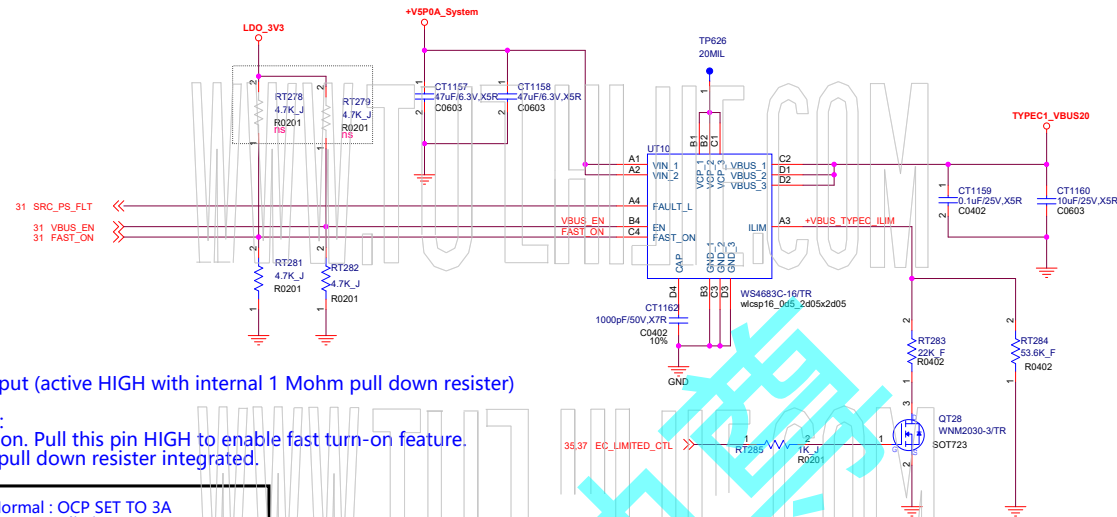
Figure 10-10 shows the connection of the four types of transceivers. The TXP and RXP pins of the transceivers are connected to the TX and RX pins of the microcontroller. The TX and RX pins of the microcontroller are connected to the TX and RX pins of the transceivers. The TX and RX pins of the transceivers are connected to the TX and RX pins of the microcontroller. The TX and RX pins of the transceivers are connected to the TX and RX pins of the microcontroller.



31 TBTA_CC1
31 TBTA_CC2



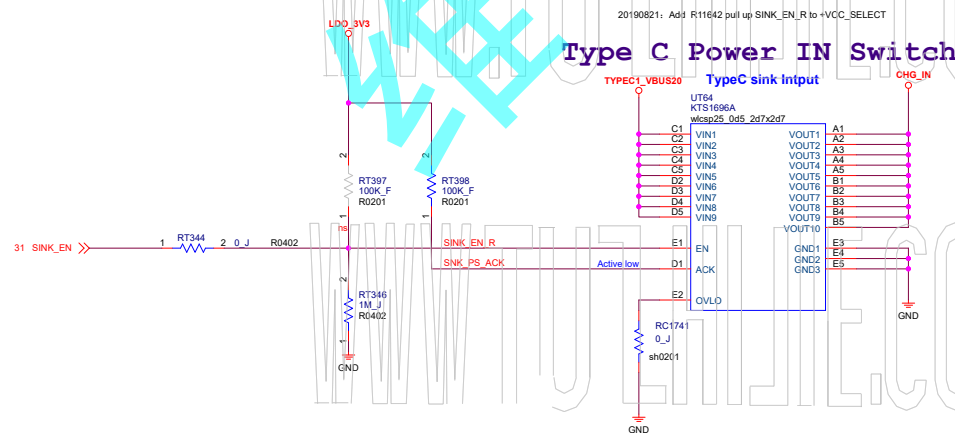
Type-C VBUS Source Power SW



EN:
enable input (active HIGH with internal 1 Mohm pull down resister)

FAST ON:
Fast turn on. Pull this pin HIGH to enable fast turn-on feature.
1 Mohm pull down resistor integrated.

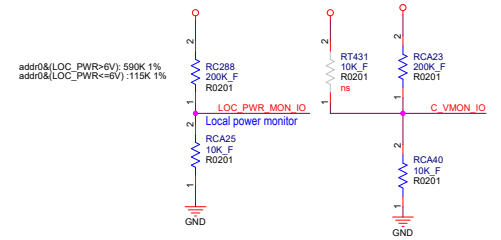
Normal : OCP SET TO 3A
Sys power limit: OCP SET TO 0.9A



Type C Power IN Switch

Slave Addr	Ra 5%	Rb 5%	
addr0:0xCC	NC	10K	<0.2V
addr1:0xCE	75K	10K	>=0.2V&&<0.6V
addr2:0xD0	33K	10K	>=0.6V&&<1.0V
addr3:0xD2	10K	10K	>=1.0V

It's is used for SMBUS slave addr0/1/2/3 setting during power on initialization.



Note:
1. Choose only one of the two parts above.
2. The left CKT above is used for SMBUS slave addr0/1/2/3 setting during power on initialization. The PDC has no ability to monitor local power when choosing this CKT.
3. Choose the right CKT above when there are requirements for PDC to monitor local power to decide if C port can source power. But the slave addr can only be set at addr0 when implement this CKT

To EC SMBUS Port1

Pin No	GPIO Mapping	Used as function
3	GPIO4	SM_CLK
4	GPIO5	SM_DATA
5	GPIO6	SM_INT
6	GPIO7	SPM_SM_CLK
7	GPIO8	SPM_SM_DATA
8	GPIO9	SPM_SM_INT
1	GPIO10	I2C_CLK_2
40	GPIO11	I2C_DATA_2
39	GPIO12	I2C_INT_2
38	GPIO13	I2C_CLK_1
37	GPIO14	I2C_DATA_1
36	GPIO15	I2C_INT_1
35	GPIO20	APU_RST_L
34	GPIO21	GPIO for customization

BITLAND 宝龙达

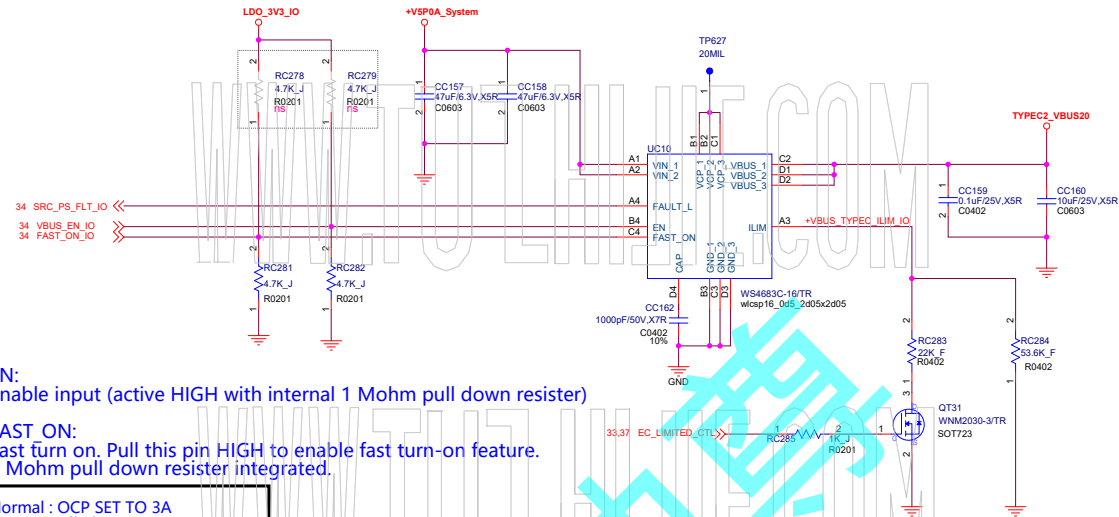
Page Name **RTS5457T**

Size **C** Project Name **S540-AMD**

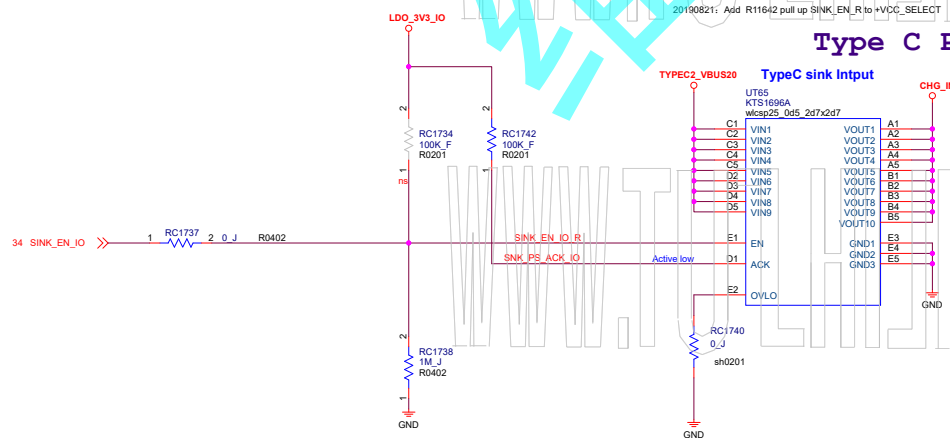
Date: Thursday, January 20, 2022 Sheet 34 of 68

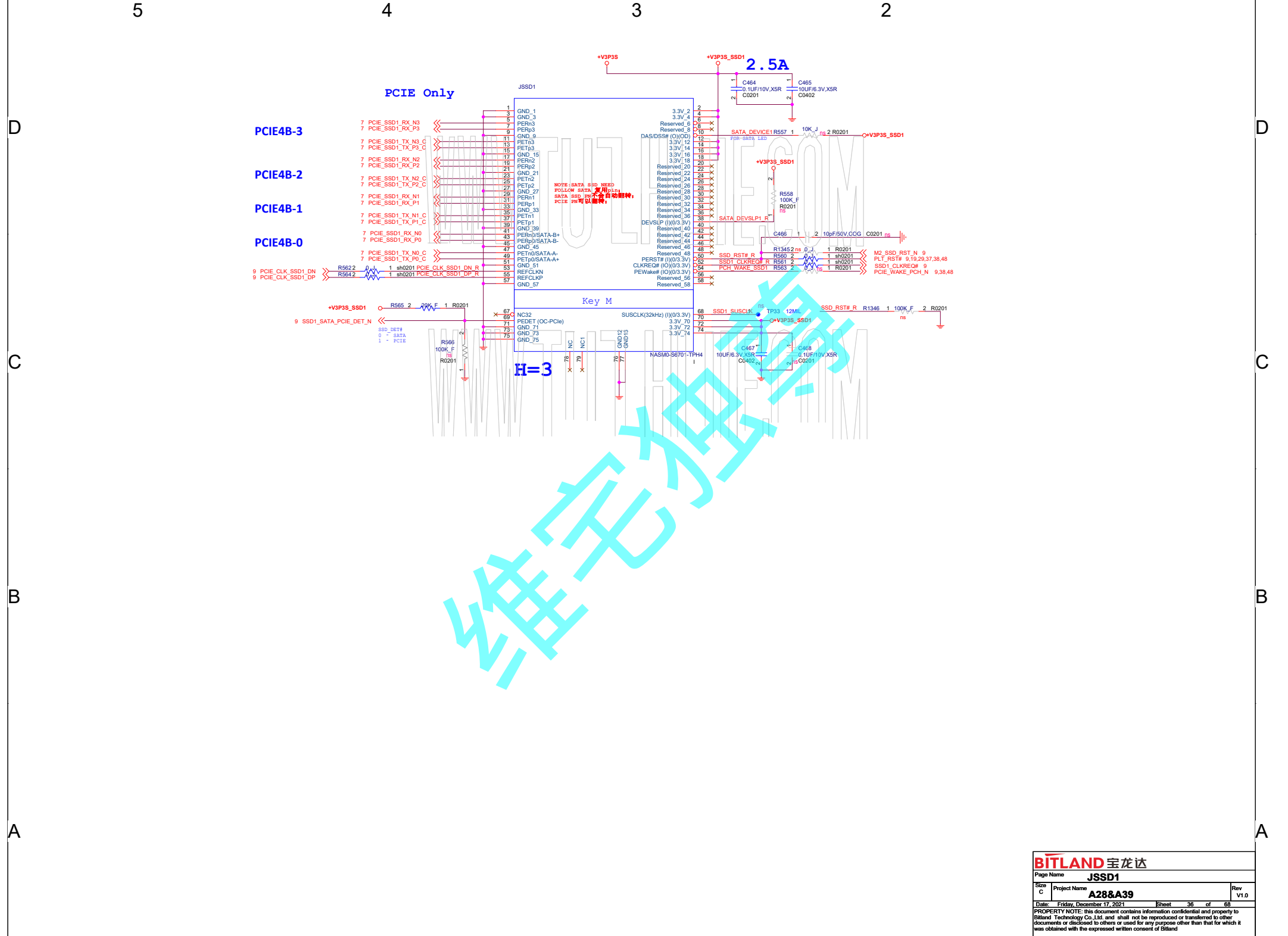
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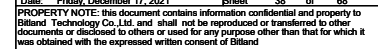
Type-C VBUS Source Power SW

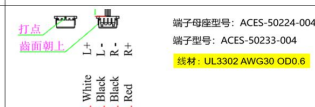
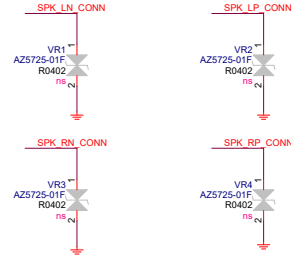


Type C Power IN Switch



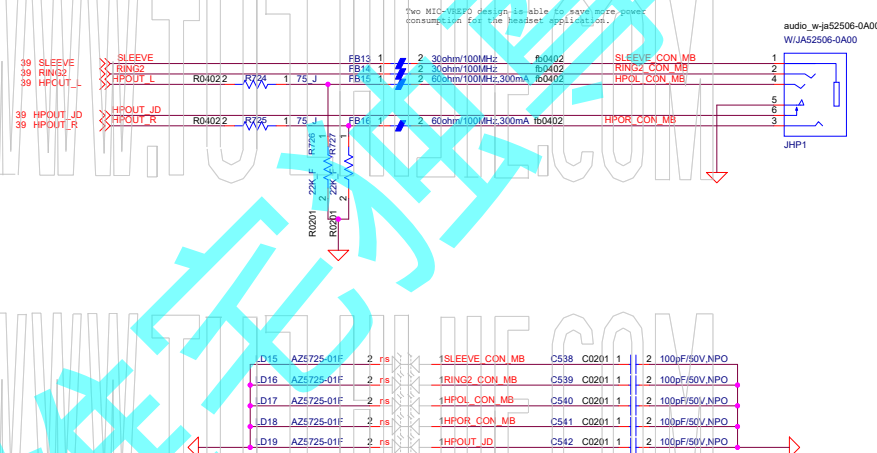
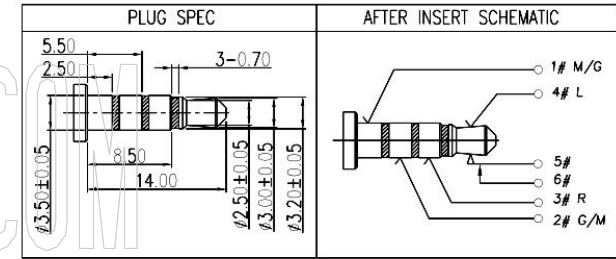


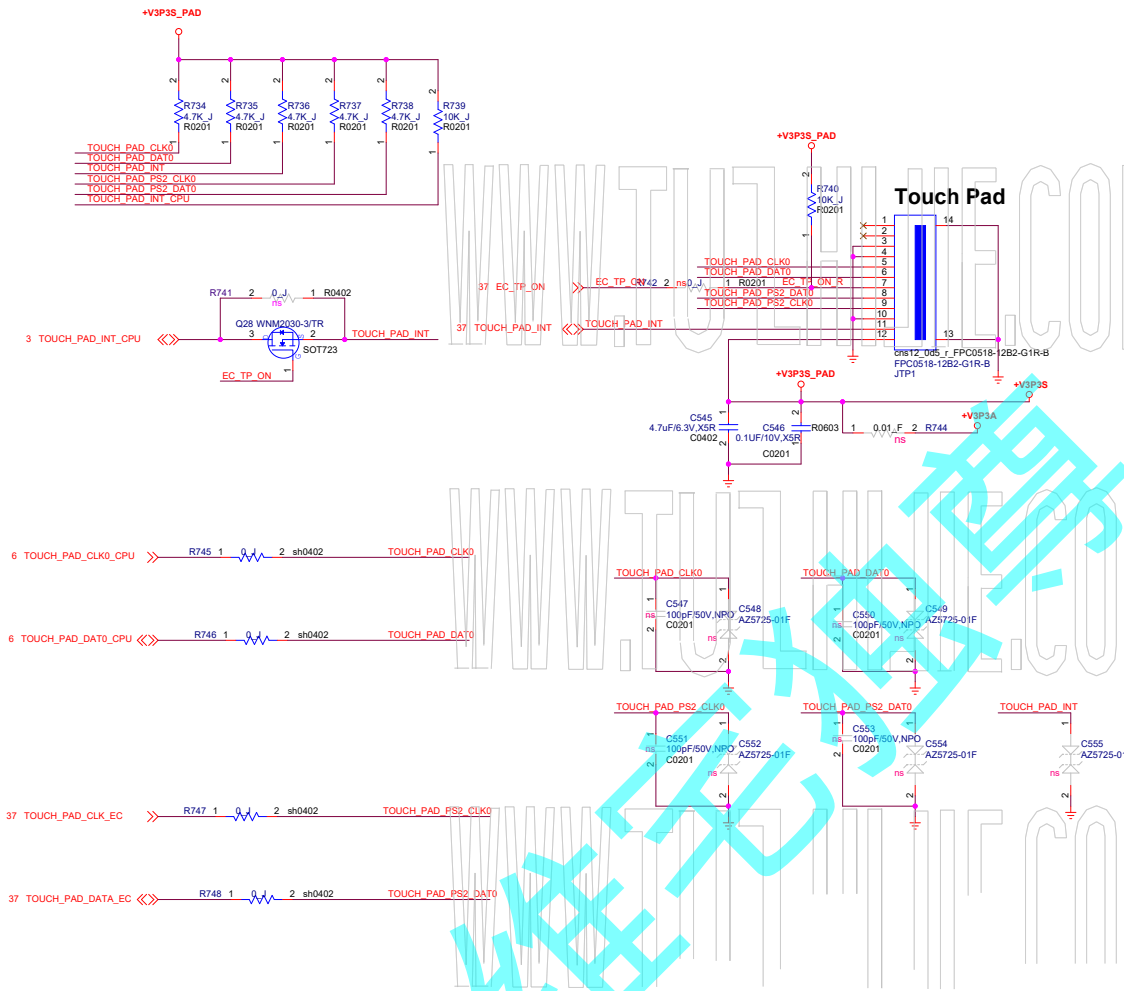




connector pin define need to follows above table for Stereo speaker, or single speaker.
Connector type could use equal solution

CODEC Output Level (Max.)	1.1 Vrms	CODEC Side
Amp Gain Setting	11 dB	Amp Side
Amp Output Power	2 Watt	
Speaker Impedance (R _{SPK})	4 Ohm	
Type value of R1 and to get R2		Type value of R2 and to get R1
R1	1.6364 Kohm	Lower than 5k ohm
R2	2.6323 Kohm	Lower than 5k ohm





Pin Assignment and Description			
Pin#	Signal	I/O	Description
1	NC		Not connected
2	NC		Not connected
3	GND	GND	Ground
4	GND	GND	Ground
5	PS2_CLK	I/O	PS/2 clock
6	PS2_DAT	I/O	PS/2 data
7	I ² C_CLK	I/O	I ² C clock I _{Drive} or I _{Sink} : 8 mA max.
8	I ² C_DATA	I/O	I ² C data I _{Drive} or I _{Sink} : 8 mA max.
9	/INT	O	Slave interrupt, low active Indicates touchpad likes to send data to system (host) when low.
10	LID_CLOSE (GPIO)	I	Indicates the lid is closed. Low: The lid is closed. High: The lid is opened.
11	VDD_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
12	VDD_3.3V	Power	

5

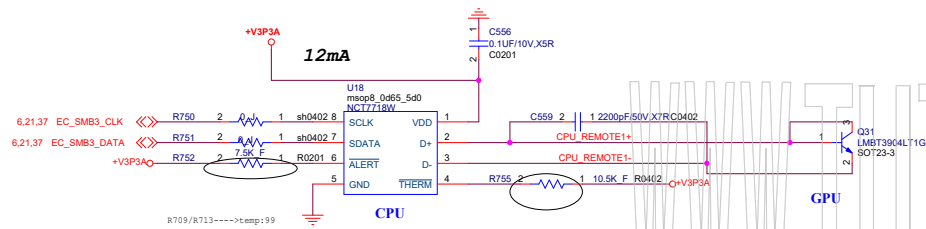
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3

2

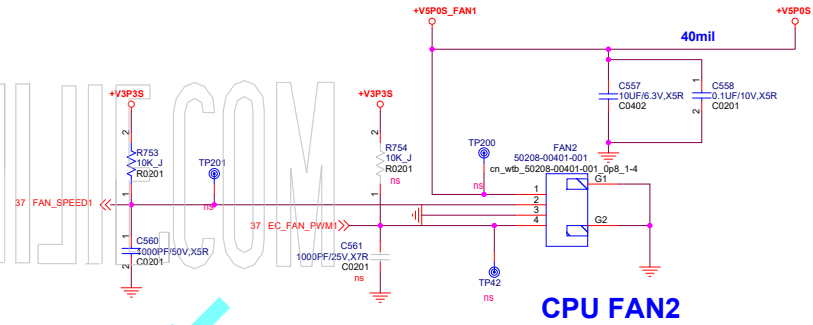
D

D



NCT7718W ADDR: 1001100xb
I2C/ SMBus™ address is 1001100xb (x is R/W bit).

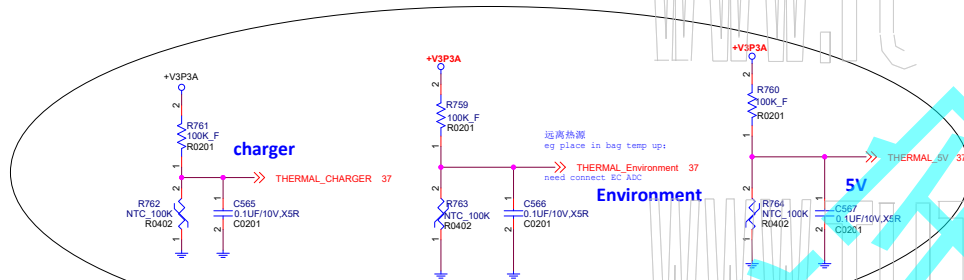
CPU/GPU use THM IC need precision temp for intel DPTF;



CPU FAN2

C

C



B

B

A

A

5

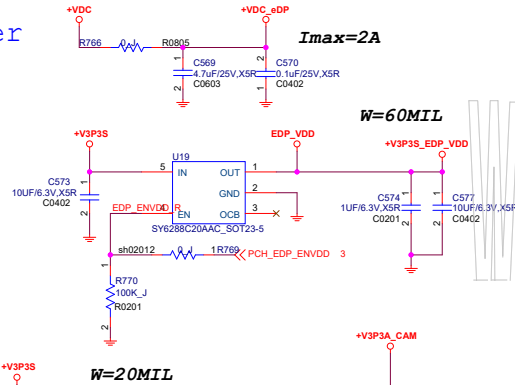
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3

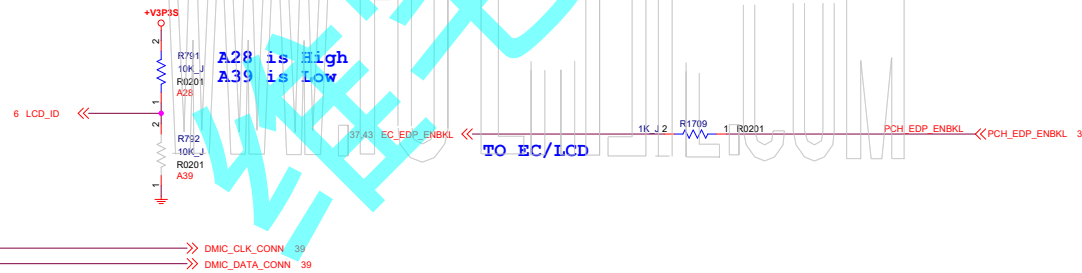
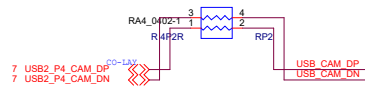
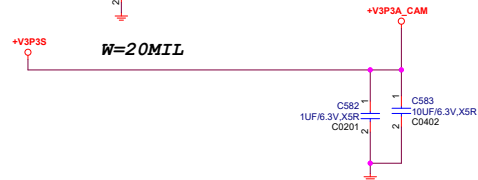
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DMIC Power

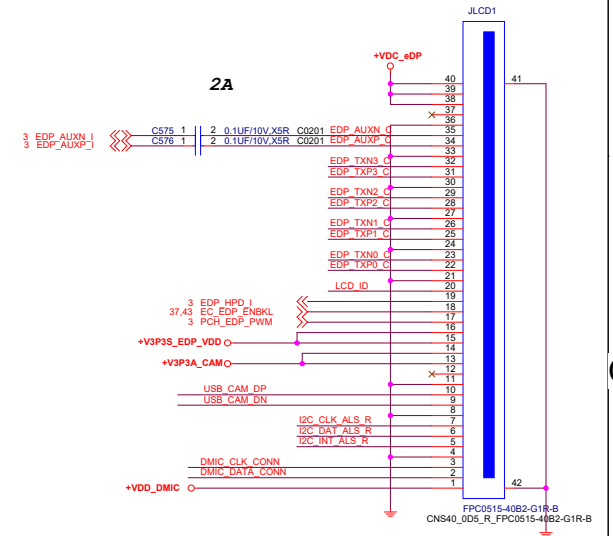
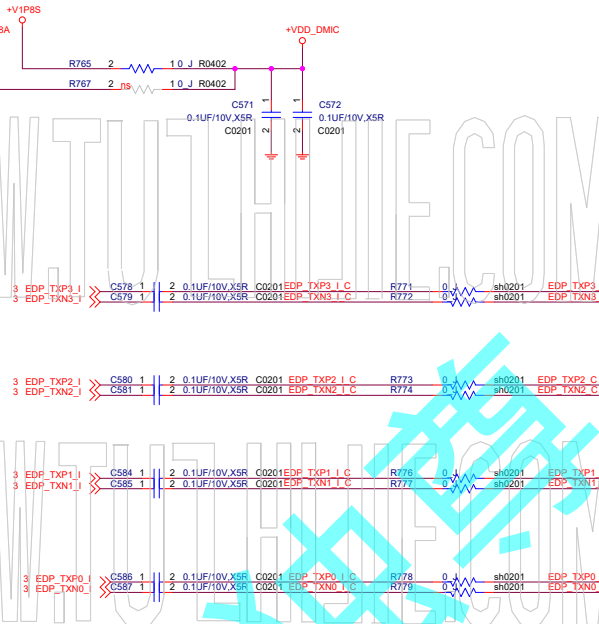
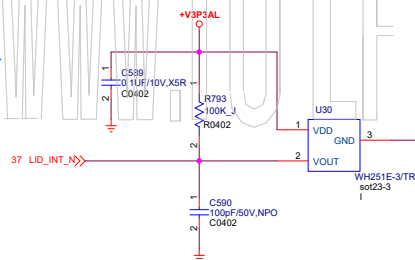
EDP Power



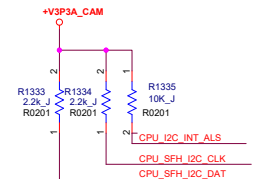
Camera

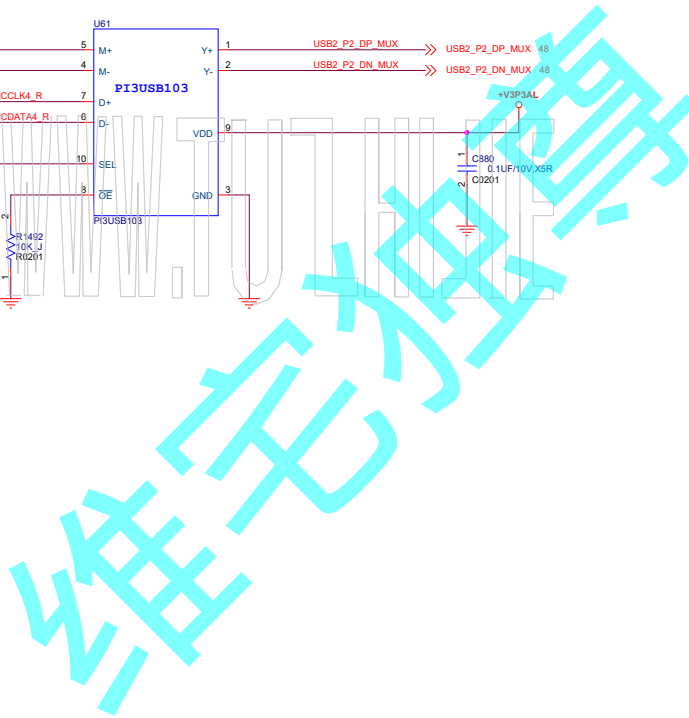


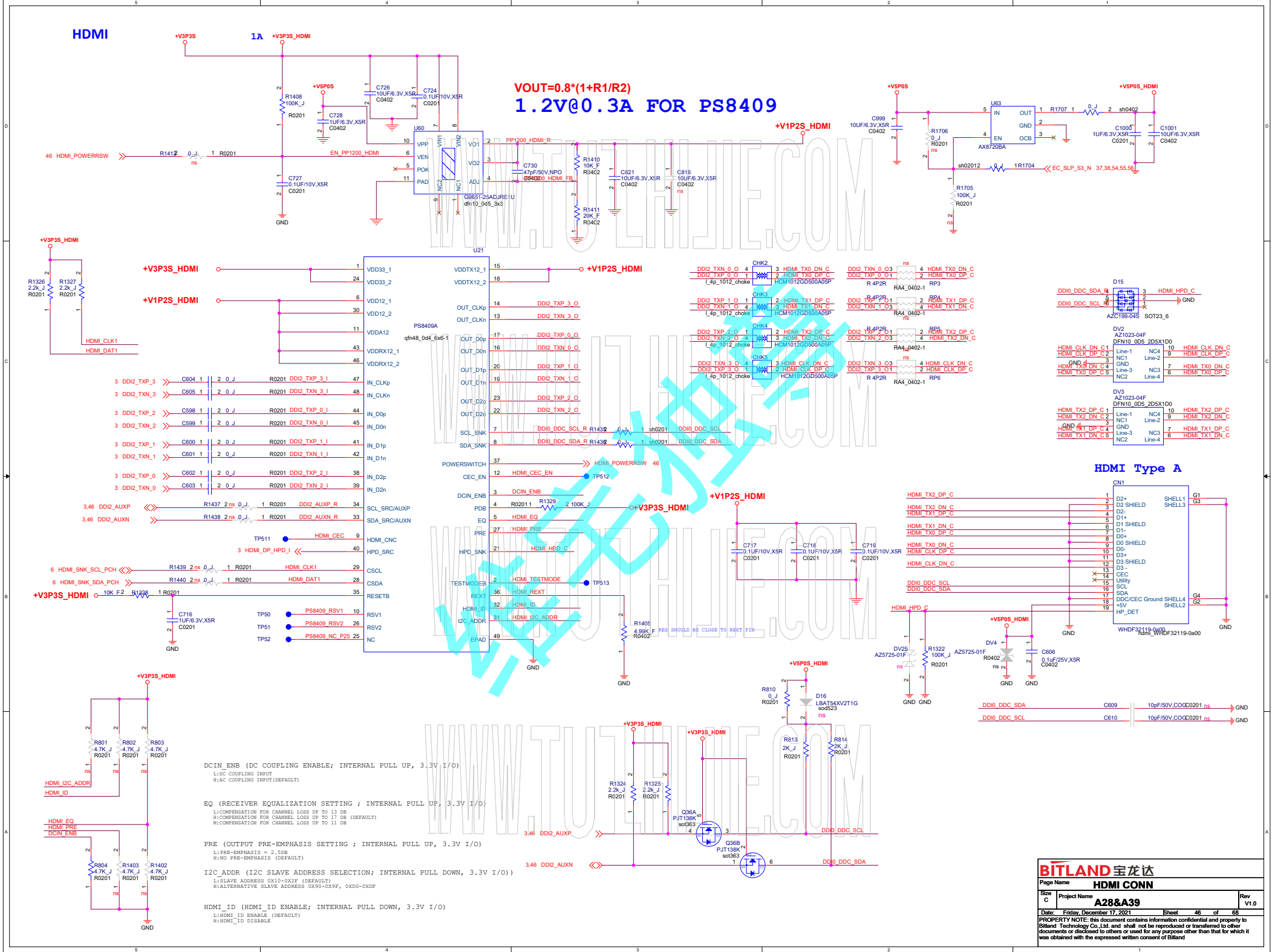
Hall Sensor

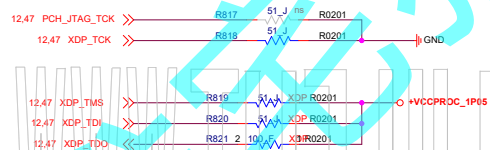
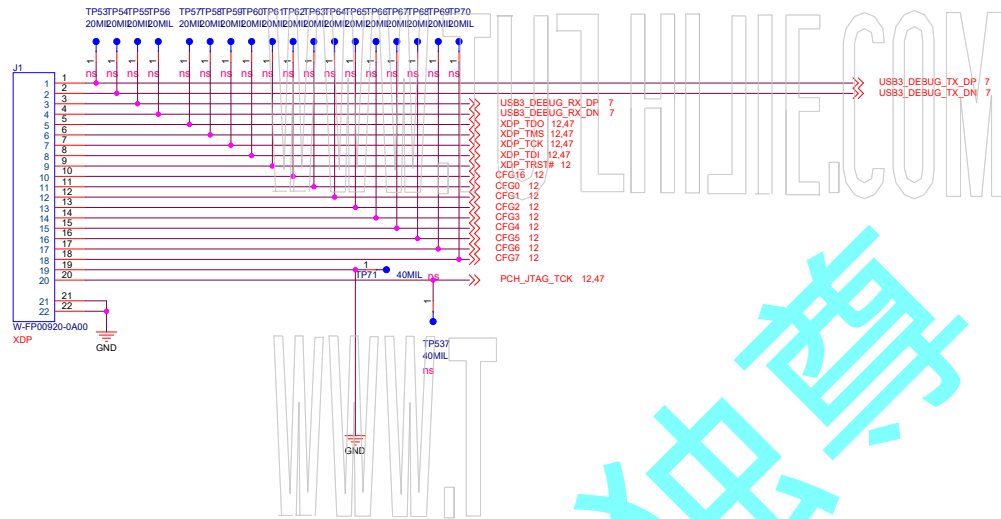


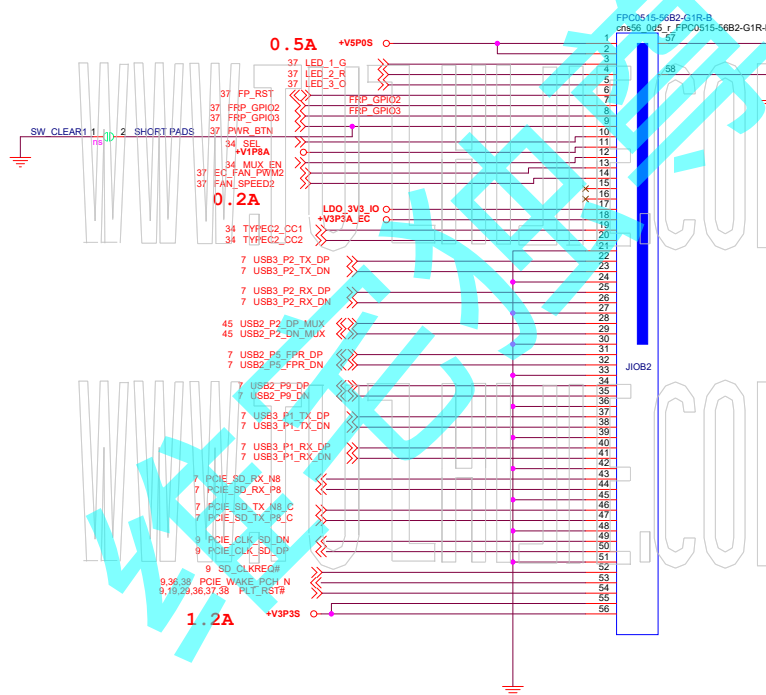
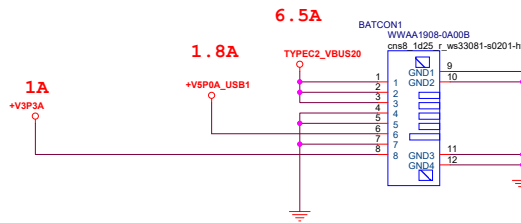
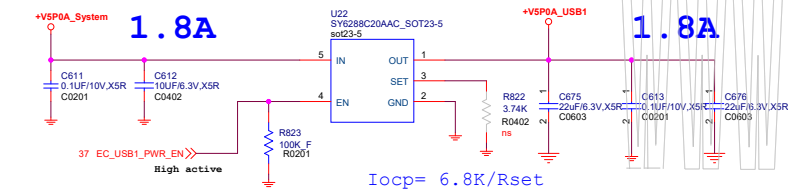
ALS

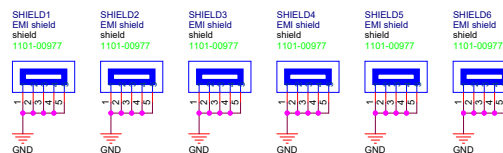
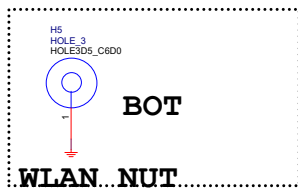




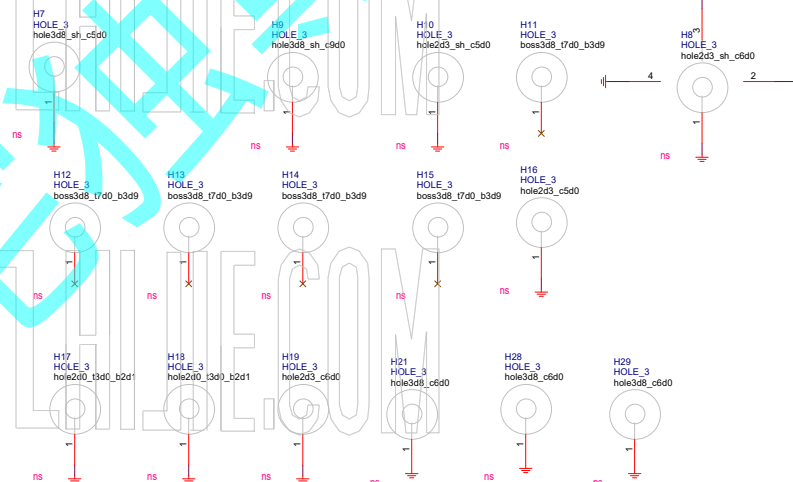
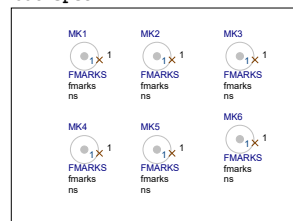






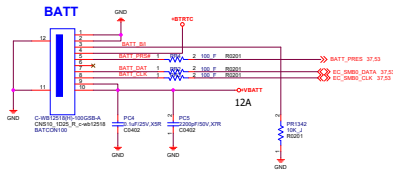


optical dot
top 3pcs
bot 3pcs

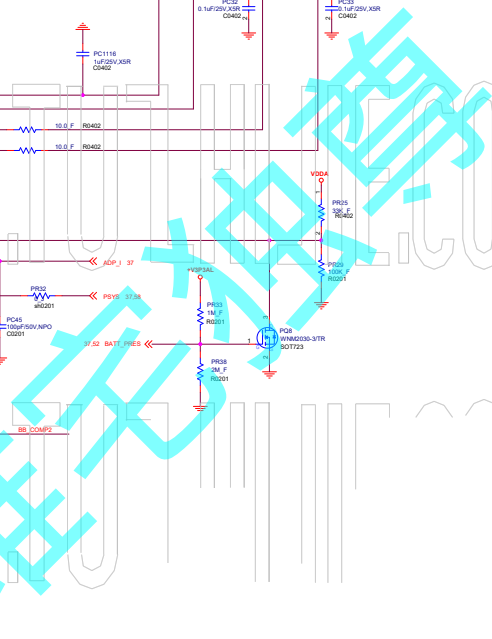


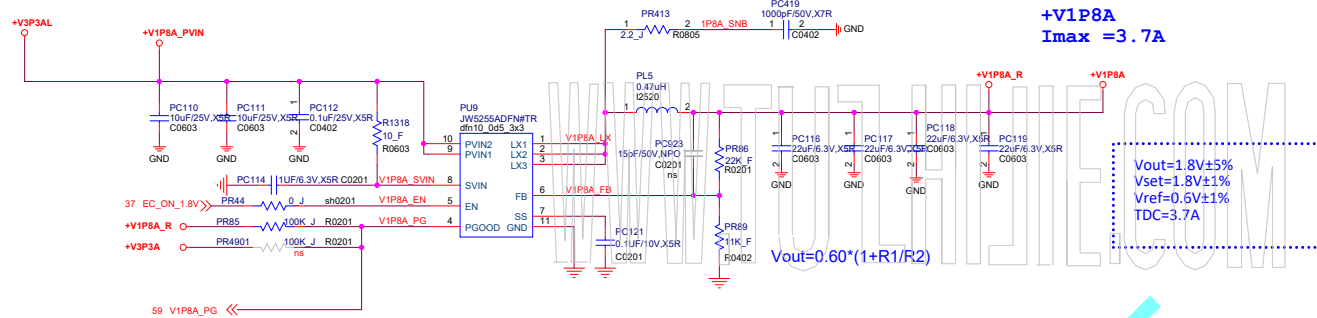
MB HOLE
not install

DCIN/BATTERY CONNECTOR



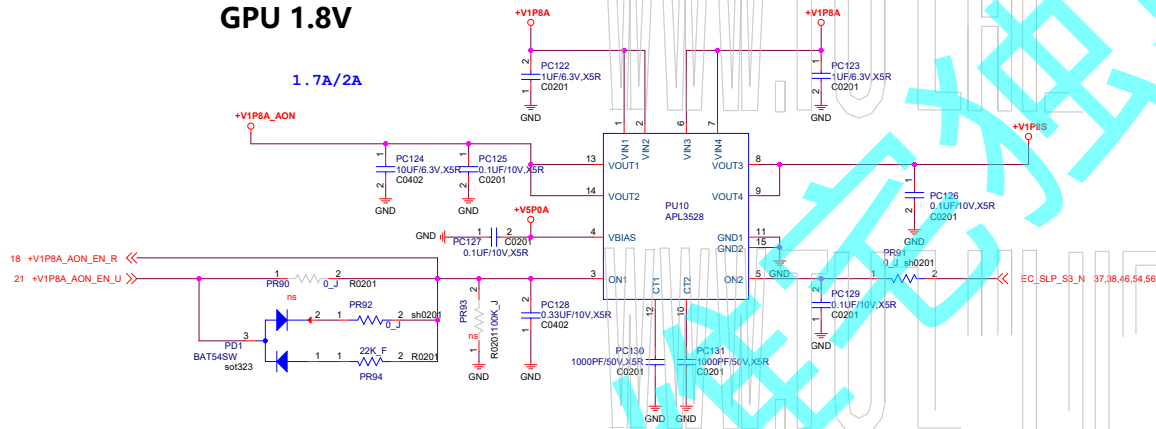
维它独尊

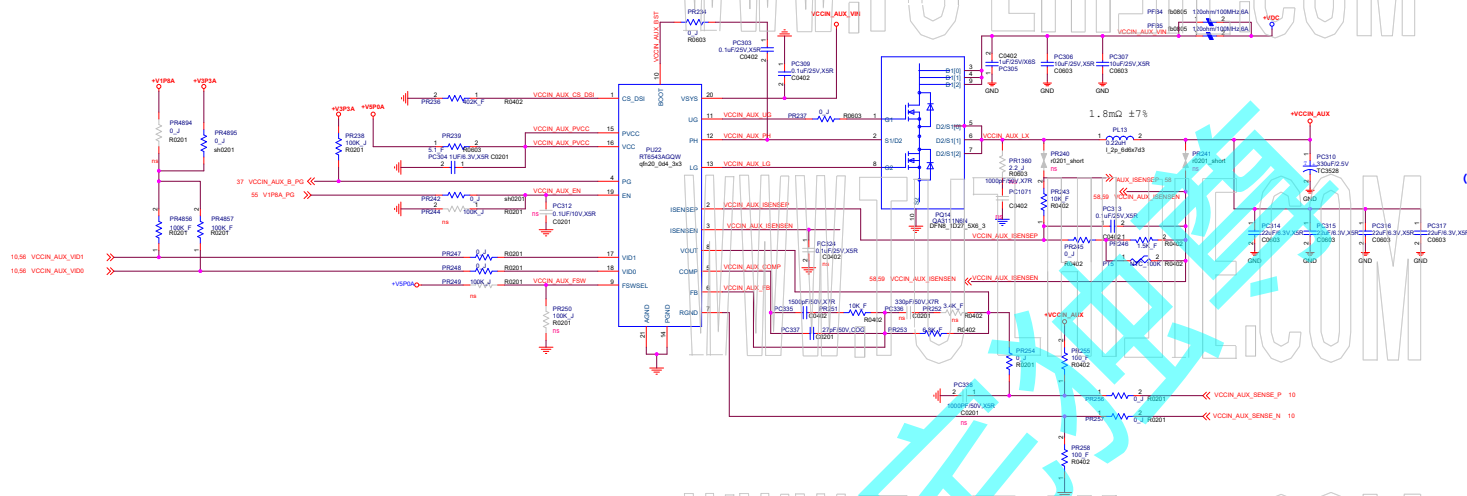




GPU 1.8V

1.7A/2A



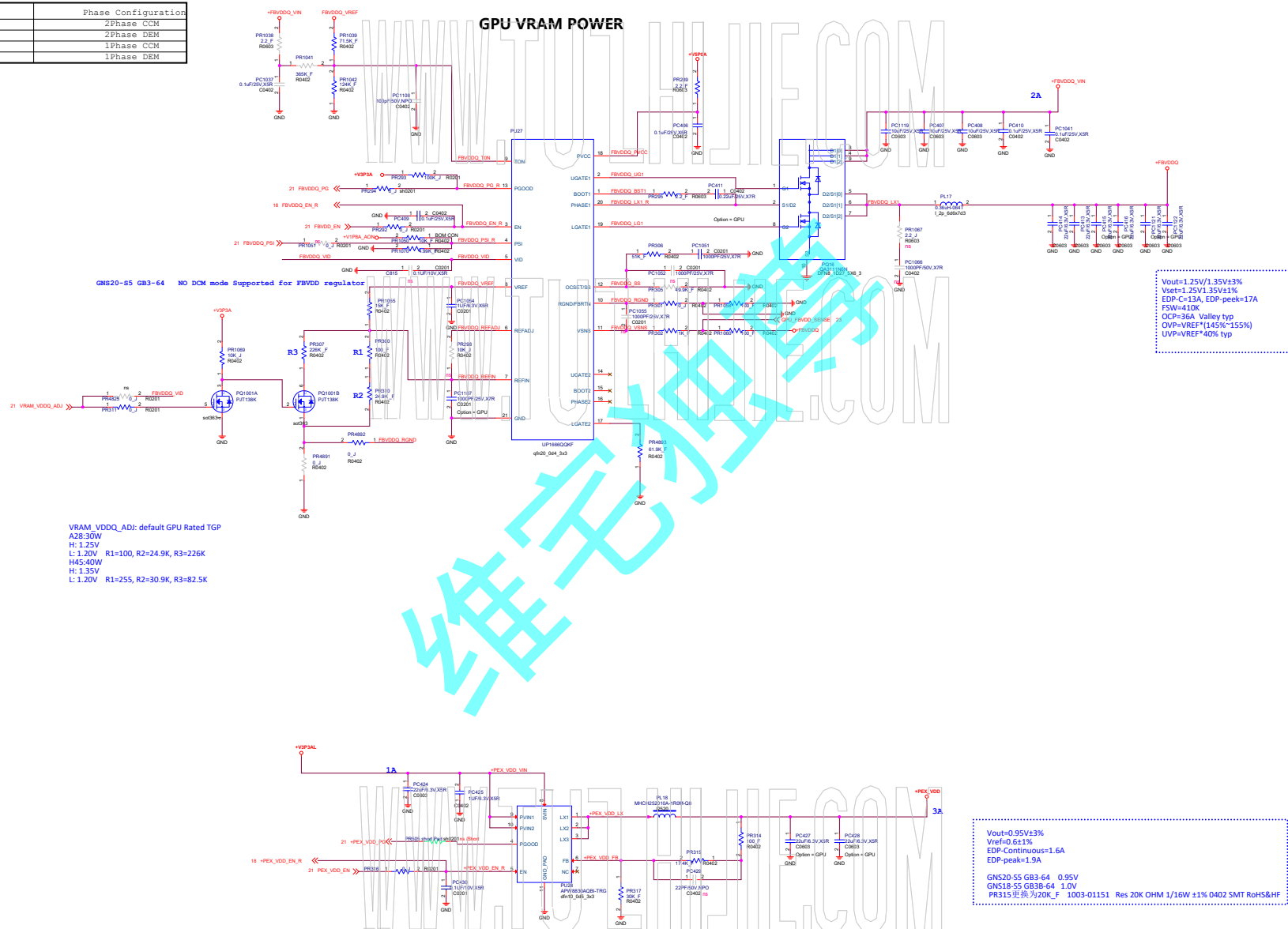


TOP side

(ADL-45W) IPL2=17A ICCMAX=34.2A

GPU VRAM
POWER

RT8816 PSI	Phase Configuration
1.6V~5.5V	2Phase CCM
1.08~1.35V	2Phase DEM
0.7~0.88V	1Phase CCM
0~0.4V	1Phase DEM



VCC_RTC
(PLT---PCH)

SRST_RST_N/PCH_RTC_RST_N
(PLT---PCH)

+VCCDSW_3P3
(PLT---SOC)

+V3P3A
(PLT---SOC)

PCH_DSW_PWR0K
(PLT---SOC)

SLP_SUS
(PLT---SOC)

+VSFOA
(PLT---SOC)

EXT_PWR_GATE#
(PLT---SOC)

+V1P8A
(PLT---SOC)

+VCCIN_AUX
(PLT---SOC)

+VCCIPOS_OUT_PCM/+VCCIPOS_OUT_FET
(PLT---SOC)

+VNN_BYPASS/+V1.0A_BYPASS
(PLT---SOC)

PCH_BSMRST_N
(PLT---SOC)

PCH_ESPI_RST
(PLT---SOC)

SUSCLK
(PLT---SOC)
AC_PRESENT
(PLT---SOC)

PWRBTN
(SOC---PLT)

SLP_S5#
(SOC---PLT)

SLP_S4#
(SOC---PLT)

SLP_S3#
(PLT---SOC)

CPU_C10_GATE_H_N
(SOC---PLT)

+VCCPROC_LP0S
(PLT---SOC)

+VDD2_CPU
(PLT---SOC)

+VCCIPB_PROC
(PLT---SOC)

VCCST_PWRGD
(PLT---SOC)

EC_VR_EN
(PLT---SOC)

+VCCIN
(PLT---SOC)

+VCCGT
(PLT---SOC)

EC_PCH_PWR0K
(PLT---SOC)

SYS_PWR0K
(PLT---SOC)

PLT_RST#
(PLT---SOC)

In NON Deep SX system sourced from same as +V1P3A

tPCRD1

tPCRD0

tPCRD7

tPCRD9

tPCRD1

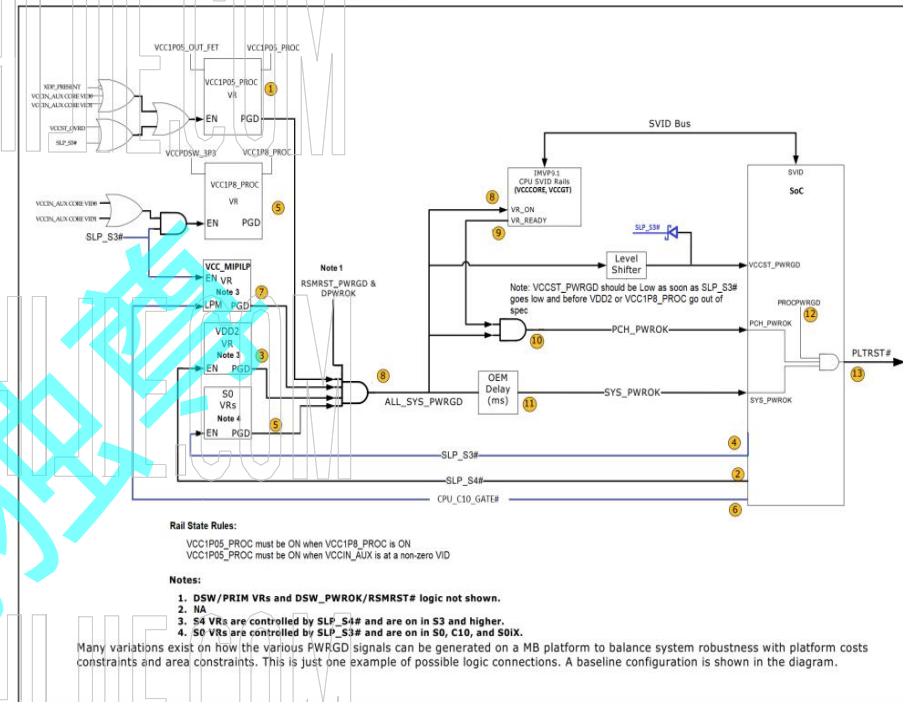
tPLTPD

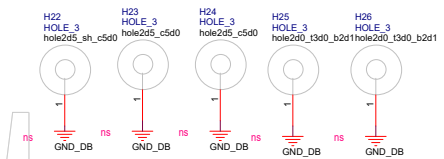
tPCRD3

(only for support Deep SX platform)

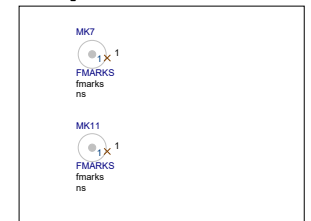
(If VNN_BYPASS and V1.0A_BYPASS are not implemented than tPCRD3 is time from VCCIN_AUX stable to BSMRST#)

Figure 519. PWROK Generation Flow Diagram





optical dot
top 1pcs
bot 1pcs



D

C

B

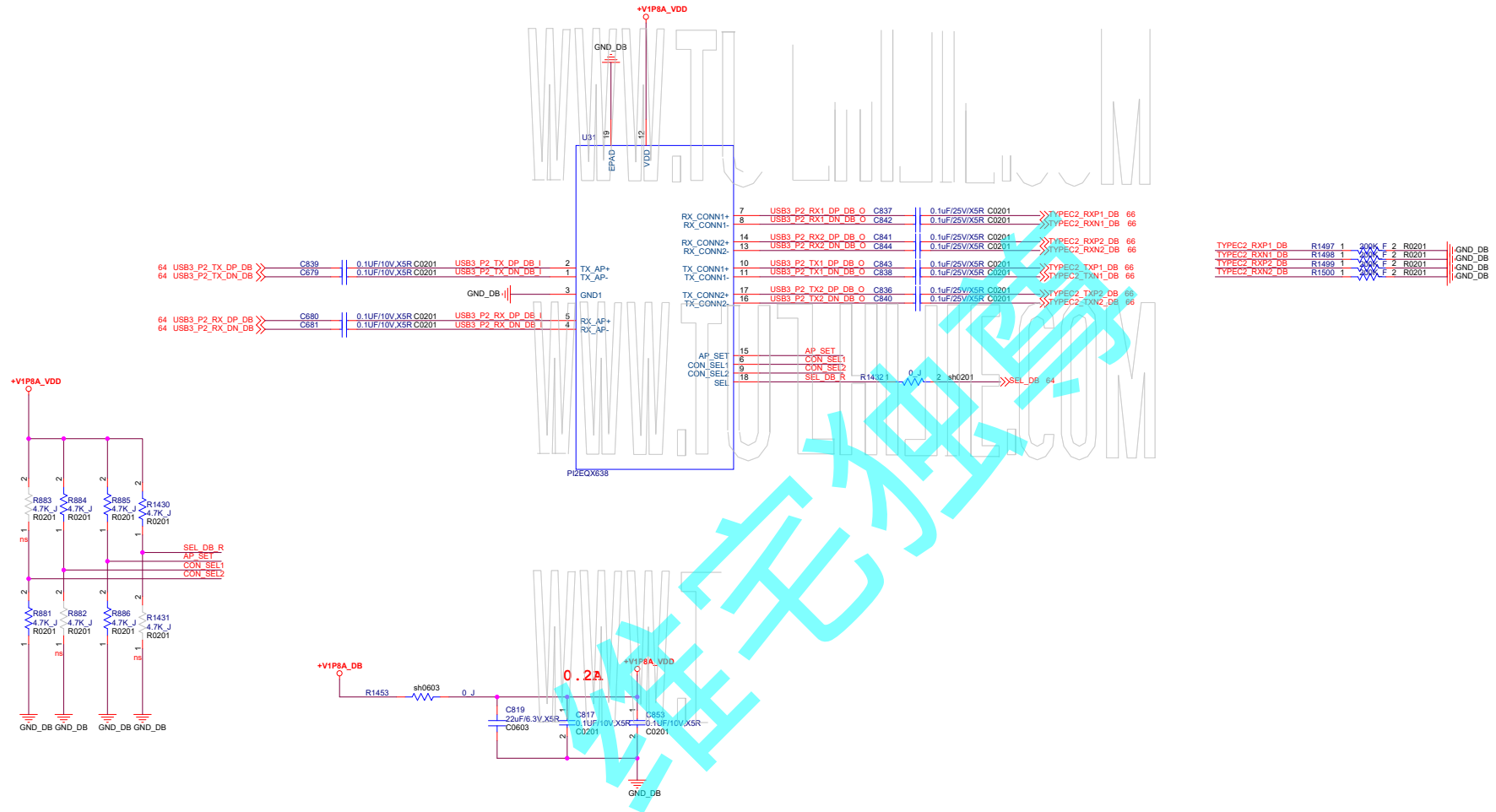
A

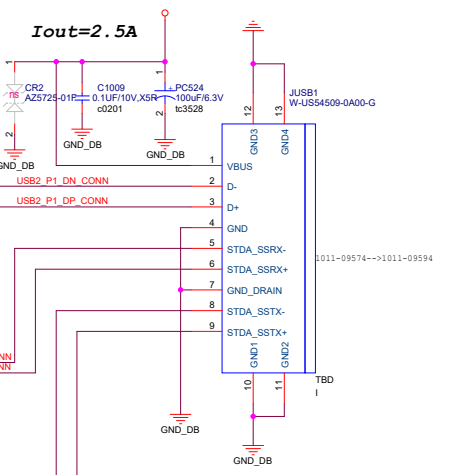
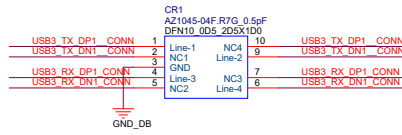
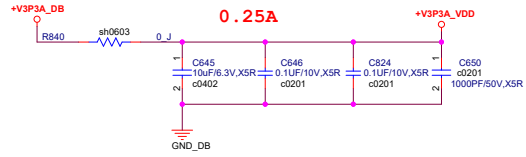
D

C

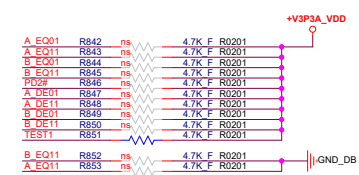
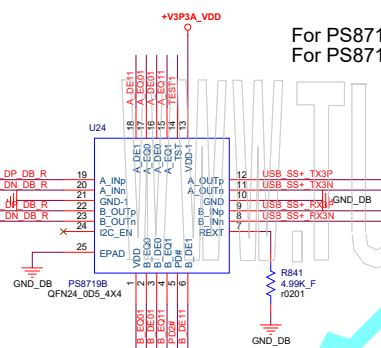
B

A





For PS8713A: VDD = 1.5V
For PS8713B: VDD = 3.3V



Equalizer control and program for channel A
3.3V tolerant. Internally pulled down at ~150KΩ
[A_EQ1, A_EQ0] ==
LL: program EQ for channel loss up to 3.4dB (default)
LH: program EQ for channel loss up to 13dB
HL: program EQ for channel loss up to 4.5dB
HH: program EQ for channel loss up to 7.5dB

Equalizer control and program for channel B
3.3V tolerant. Internally pulled down at ~150KΩ
[B_EQ1, B_EQ0] ==
LL: program EQ for channel loss up to 3.4dB (default)
LH: program EQ for channel loss up to 13dB
HL: program EQ for channel loss up to 4.5dB
HH: program EQ for channel loss up to 7.5dB

LFPS swing adjust.
3.3V tolerant. Internally pulled down at ~150KΩ.
TEST ==
L: Normal LFPS swing (default)
H: Turn down LFPS swing

Programmable output pre-emphasis level setting for channel A
3.3V tolerant. Internally pulled down at ~150KΩ
[A_DE1, A_DE0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 2.7dB de-emphasis
HH: 5dB de-emphasis

Programmable output pre-emphasis level setting for channel B
3.3V tolerant. Internally pulled down at ~150KΩ
[B_DE1, B_DE0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 2.7dB de-emphasis
HH: 5dB de-emphasis

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